Advanced Electron Beam Nanoprobing Techniques for Electrical Characterization and Fault Isolation
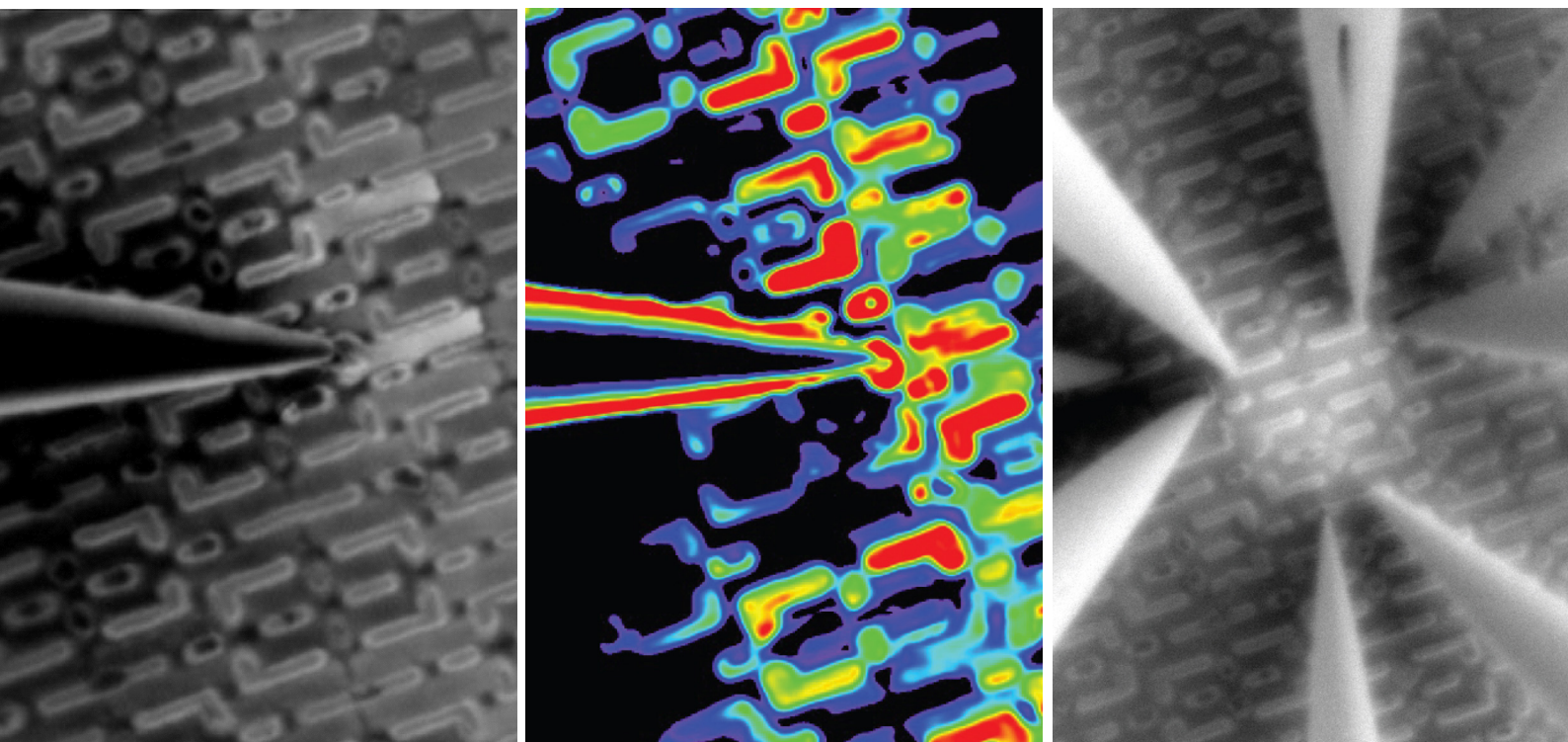

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In situ EBIC Measurements of IGBT During Device Turn-on

Seeing beyond

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Abstract

A simple method for the *in situ* examination of device turn-on in an insulated gate bipolar transistor (IGBT) is presented. A Ga[+] focused ion beam (FIB) was used to mill away a wedge-shaped section from the material so as to leave the exposed devices operable by the surface gate and emitter contact pads. Through this window, a series of nanoprobing-based measurements were undertaken. Sensitive, electron beam induced current (EBIC) measurements strongly delineated both of the *p/n* junctions in the exposed surface, both those between the N[+] emitter and the P- well or body, and between this P- body and N-drift region. Next, the gate voltages were varied and a series of EBIC images were taken of the body/drift depletion zone. Quantitative plots of the same gave an indication of when the insulated gate portion of the device turned on. Finally, a follow-up experiment showed the effect of applied bias on active voltage Ccontrast (AVC) of the junction. The results point to a method for examination of junctions and their behavior under gate bias with very little sample preparation. The results also ease some concerns about the use of GaFIB in sample prep for junction examination in failure analysis, given the detailed work that was possible.

Introduction

Power semiconductors are key components for transportation, electrical grids, induction heating, wind turbines—even robot welding machines [1]. These devices are valued for their properties of high efficiency, high currents, and fast device switching [2,3,4]. Power devices are required to handle very high currents and voltages, and some failure mechanisms involve hot carriers in the depletion zone [5,6]. Therefore, the complete understanding of junction profiles and performance will be critical to the disciplines of failure analysis, device tailoring, and manufacturing line monitoring.

An insulated gate bipolar transistor (IGBT) is a three terminal device that acts as a switch. It is a cross between a conventional bipolar junction transistor and a MOSFET and is shown in Figure 1. It is a vertical transistor in that when the device of the insulated gate transistor is turned on, a bipolar transistor allows current to flow through the sample. The device is turned on by first turning on the MOSFET, and then then holes may turn on the internal PNP bipolar transistor. It's a massive parallel device, with gates laid out in a fishbone pattern [7]. Because it is a vertical transistor, it introduces challenges in any FA technique that needs to look below the surface [8].
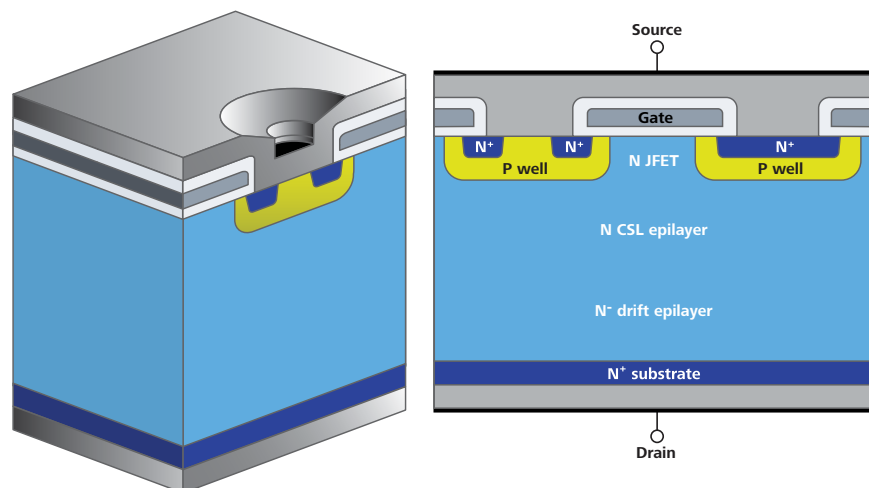

Figure 1 Cross-sectional diagram of an IGBT chip. The views are shown in both a 3D fashion (left) to highlight the structure of the gates, and in 2D to highlight the vertical conduction path through the sample.

The temperature dependence of leakage in Si-based IGBTs has been cited as a reason for their limitation compared to other power devices [9]. Thus, the IGBT presents several challenges for failure analysis [10].

The EBIC technique for evaluation of *p/n* junctions has been widely studied [11-18]. EBIC is driven by internal electric fields that exist at the depletion zone of a *p/n* junction. If an electron absorbs sufficient energy, it may be promoted to the conduction band (See Figure 2, top), and the event is said to create an electron-hole pair. Then the electric field acts on the charge carriers, and this movement of charge may be detected as EBIC by the placement of a probing needle in the appropriate location, as shown in Figure 2, bottom. As implied by the band shape, this only takes place at the middle of the junction, at the depletion zone. The field is also a vector quantity, oriented normal to the surface of the *p/n* junction.

Electron-hole Pair Creation
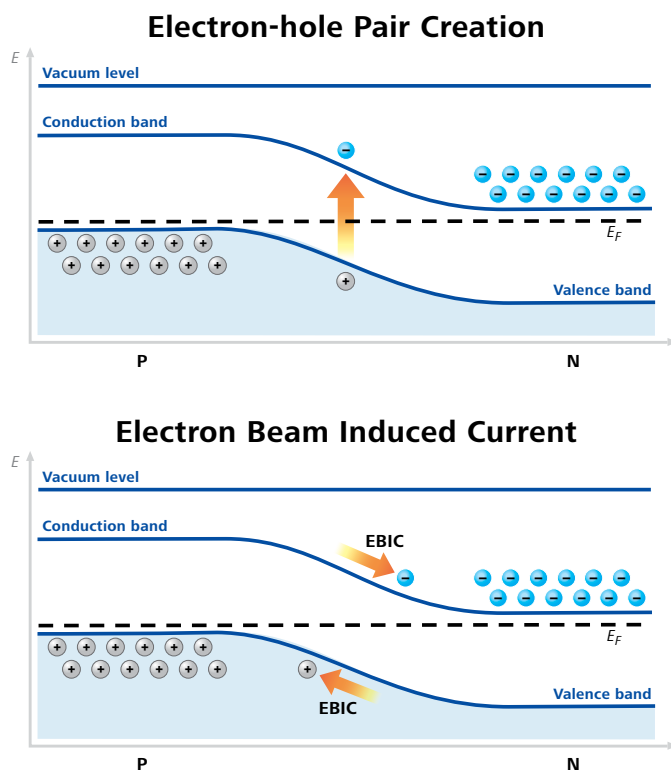

Electron Beam Induced Current

Figure 2 Band diagram for a p/n junction. Top image depicts electron-hole pair creation. Bottom image shows charge carrier movement due to the electric field at the p/n junction, known as EBIC.

Procedure

A. Sample preparation

A commercially available IGBT chip was cross sectioned. Various steps in the procedure are depicted in Figure 3. The chip was glued with silver paste to a 12.5 mm aluminum SEM specimen stub. Sputter coating was used to coat the sample with 20 nm of gold. A beveled cross-section was cut across 12 gates in the central area of the device with the focused Ga+ ion beam (Ga-FIB) of a ZEISS Crossbeam 350 FIB-SEM instrument. In this process, a 330 µm x 70 µm rectangular FIB shape was used to mill a trench into the untilted sample at 30 kV with 30 nA FIB current for approximately 6 hours. Since the FIB column was oriented at 36° to the horizontal, the opening thus created measured approximately 330 µm x 100 µm on the sample surface. Because FIB cuts tend to show a beam current and material dependent angular offset from the beam incidence, the cross-section was oblique to the sample surface at approximately 34°. The cross-section was then polished at 30 kV with a 3 nA beam using a 330 µm x 5 µm rectangular FIB shape for 2 hours, resulting in a final cross-section angle of approximately 35° to the sample surface. Figure 3, upper right and lower left, show top-down SEM views of the final cross-section, obtained in the same instrument. Although the cross section had some vertical FIB milling 'curtaining' artifacts due to the relatively high beam current used for polishing, the passive voltage contrast between p- and n-doped regions stand out using the in-column secondary electron detector of the ZEISS Crossbeam (Figure 3, lower right).
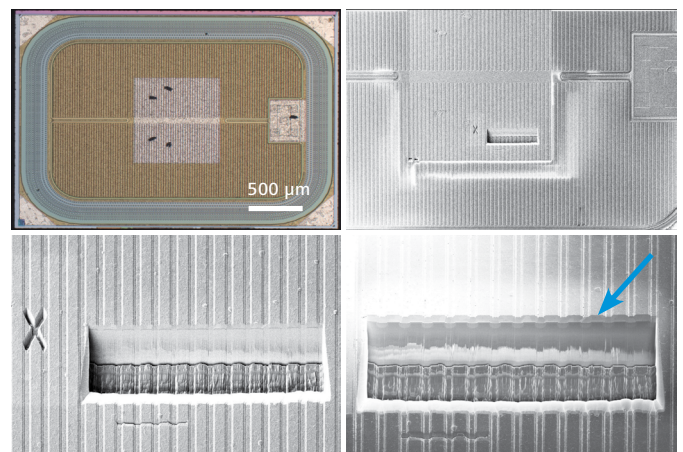

Figure 3 Views of the IGBT chip used in this experiment, and the FIB trench cut into it. Upper left: light microscopy image of the chip before milling. Upper right: SEM image of the location of the trench relative to the visible structure on the chip. Lower left: cut into the structure. Lower right: In-column secondary electron detector SEM image to show the as-cut structure. Already some voltage contrast on the implant regions is visible (blue arrow).

B. EBIC analysis

The sample was then examined with a Kleindiek Nanotechnik PS8e Prober Shuttle setup which included an EBIC amplifier, and inserted into a GeminiSEM 300 field emission SEM for imaging and stimulation with an electron beam. The geometrical relationships between the Ga+ beam used for milling in the FIB, the tested surface, the nanoprobing needles, and the window examined is shown in Figure 4.

For the analysis, the measuring probe was placed on the large emitter pad on the top surface of the chip. The chip design essentially makes a large area on the top surface into a giant contact pad for all of the device's emitters. This pad can be seen as the silver square with four probe scratches in Figure 5. Thus, any EBIC current in the system that makes it to the emitter is imaged using this setup.
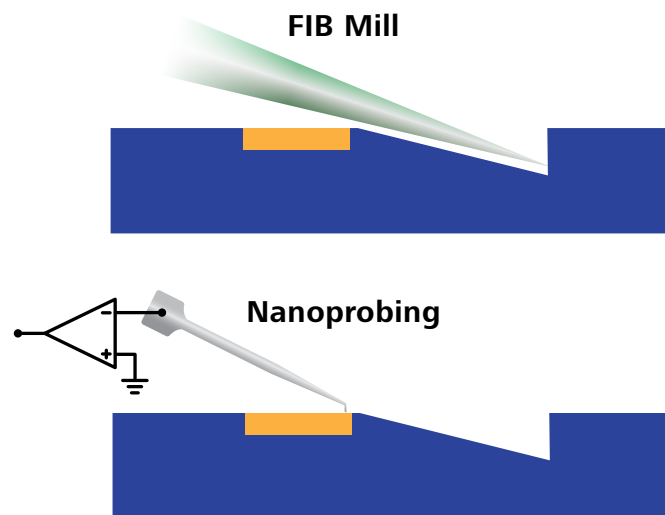

Figure 4 *Comparison of the geometric relationships between the FIB milled window and the nanoprobing setup. The green cone represents the FIB beam, and the test pad is shown as a gold rectangle.*
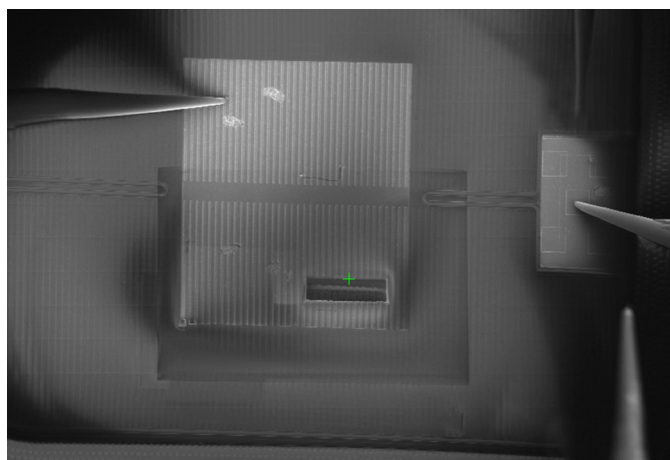

Figure 5 *SEM micrograph at 5 kV showing the FIB wedge cut and probes on the emitter and gate pads of the device.*

Results

A. Cross section and PVC

The exposed surface in the FIB-milled window was examined at high magnification by SEM. Various contrast areas were noted. A comparison of the passive voltage contrast (PVC) of the *p/n* junctions in the sample is shown in Figure 6. The cross-sectional technique has empowered strong PVC delineation between the N+ emitter, P- body, and N-drift regions of the sample. All of these regions yield quite strong PVC despite the surface having been prepared with a GaFIB beam. The apparent depth of the features are exaggerated by virtue of the fact that this is looking at effectively infinitely long features projected onto a surface at an angle of 35° relative to the chip's normal surface.
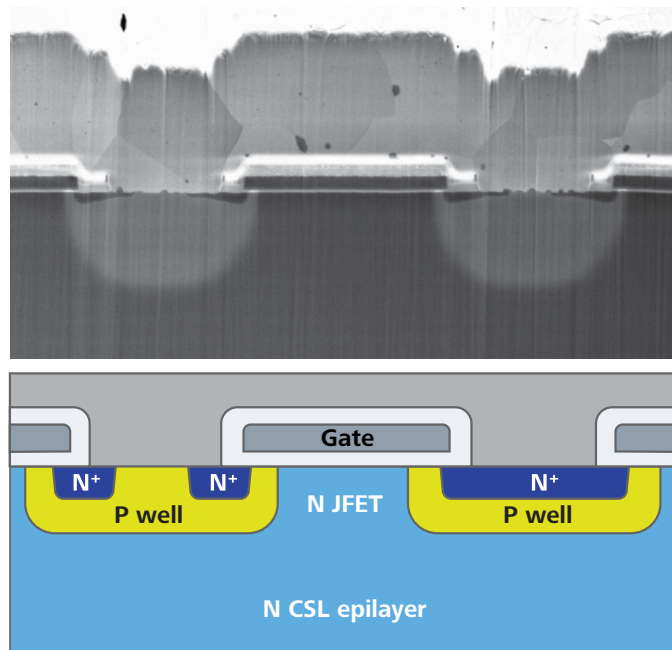

Figure 6 *Comparison of the SEI views of the devices in the sample against the layout of a typical IGBT device.*

B. EBIC results

Various EBIC measurements were made through the window at acceleration potentials ranging from 0.9 kV to 2.0 kV, with a 60 μm SEM aperture. The relationship between the outer surface metallurgy and our exposed window may be easier to understand by considering Figure 7. The depth of the FIB mill only extends about ten microns below the depth the P- body shapes. As such, the only depletion zones that would be exposed in the sample are those in the N- drift region. One can clearly see a strong EBIC signal from about a dozen "smiles", which appear to be associated with the P-body shapes. This signal is detected despite the use of GaFIB in the sample preparation.
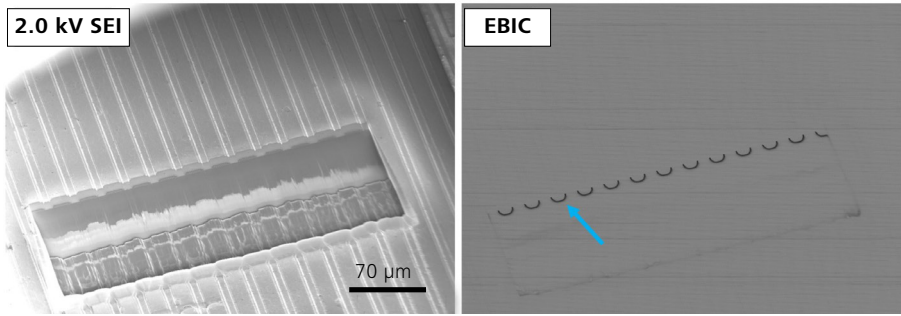
Figure 7 *Comparison of the secondary electron and EBIC images of the FIB wedge exposed area in the sample. With a viewing angle normal to the surface, the depletion regions are crisply seen, even at an oblique angle. The blue arrow points to one such depletion zone.*
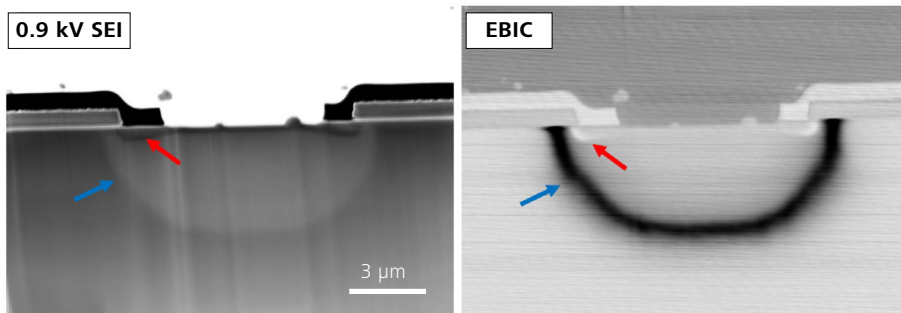

Figure 8 *High magnification views of the space between two gates of the IGBT cross section, taken at 0.9 kV. The red and blue arrows highlight two different implant zone interfaces in both images. Left: passive voltage contrast (PVC) in SEI image shows implant types. Right: EBIC image highlights the depletion zones between the two various implants. Note the variation in width and polarity between the different types.*

It should also be noted that some types power semiconductor devices are built on rotated wafers, such that their natural cleave planes are at a 60° angle to the printed features. Thus, achieving any polished cross section which is normal to the devices would prove to be extremely difficult. In this operation, FIB milling patterns may be drawn at any desired angle.

Closer examination with EBIC and SEM examination, at higher magnification in the area between two gates is shown in Figure 8. Even though the exposed surface is at approximately 35° angle to the surface normal, depletion zones are easily measured. These results highlight a major benefit of this work, in that it is possible to pick an area on the surface of the sample, and examine *p/n* junctions there, without major deterioration of the device.

In the EBIC image, there are now two depletion zones visible, not only the depletion zone between N- drift and P- body "in black" but also that between the P- body and N+ emitter, seen as a small white band in the right side of the Figure. The opposite polarities of the EBIC responses may be explained by the opposite orientations of the two electric fields, *n/p* and *p/n*. One field would drive carriers toward the needle (white signal), and one would drive away carriers toward the it black signal against a grey background). The extent, shape, and magnitude of the body/drift zones in this work are quite similar to previous work where EBIC measurements were taken directly off of cleaved samples [19, 20]. The importance of optimizing beam conditions and scan speed for this type of device has been reported previously [21].

This work builds on that paper [21] to evaluate the capabilities of observing changes in depletion zones by means of manipulating the IGBT's gate voltage.

C. Manipulation of gate voltage and MOSFET EBIC

The next set of experiments involved measuring EBIC at the emitter pad, under stimulation of a 0.9 kV SEM beam, while at the same time, incrementally varying the gate voltage on the gate pad, in a range from -4.0 V to +4.0 V. A sampling of the results is shown in Figure 9. Once again, both types of depletion zones are visible. It was decided however to concentrate on conditions which would optimize the "smile" of the P- body to N- drift region, the one that would be critical to device turn-on. In the measurement series, at negative voltages, the depletion zone becomes slightly wider, darker (meaning more negative currents) with increasingly negative voltage. However, as the voltages cross into positive territory, the depletion zone fades into non-existence. This is to be expected, as the inversion of this channel must occur in order to allow current to flow from top to bottom of the device. This is the stage in device switching that relates to the turn-on of the insulated gate portion of the transistor. This result of a uniformly inverted channel, all the way across the "smile", should be expected from physics, but is not what is typically shown in most sketches in tutorials as to what occurs upon device turn-on. These seem to imply the only conduction path would be immediately underneath the gate. In contrast, the results presented here show that the whole depletion zone inverts as the gate is biased positively. In this regard, the authors highlight this finding as a likely novel and important contribution to the operation of IGBT turn-on.
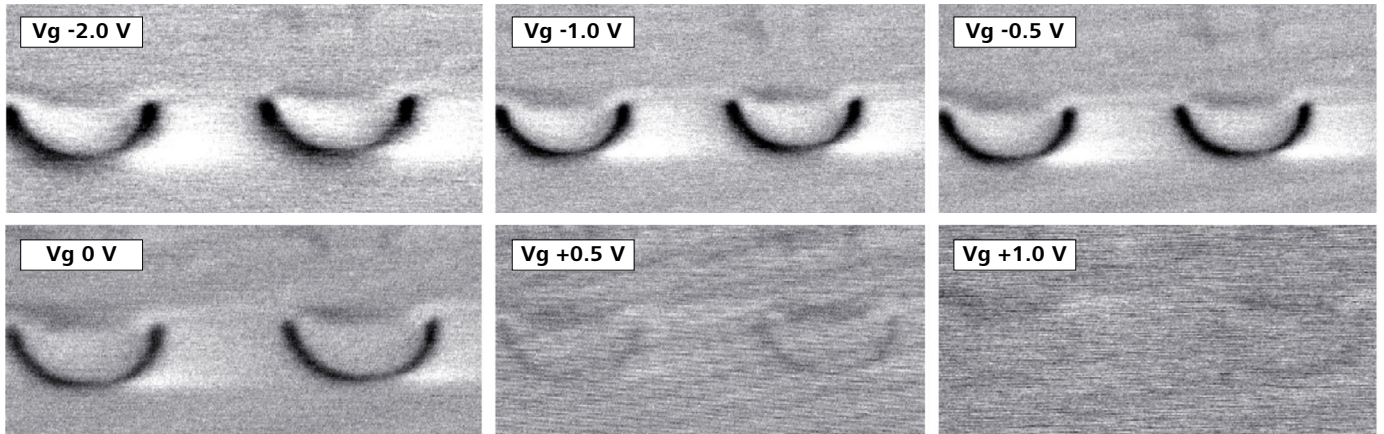
Figure 9 EBIC images of the depletion zones between the P- body and N- emitter as a function of gate voltage.

A quantitative treatment of the above EBIC current measurements as a function of gate voltage is further explored in Figure 10. A line profile was drawn across the upper edge of the "smile" of the depletion zone (see green box), and an average of 8 pixels' worth of data are reported for every point on the graph. At a gate voltage of 0.0 V, (blue dotted line), a distinct depletion zone is seen. As negative voltages are applied, −0.5 V and −1.0 V, the depletion zone gets wider and more distinct. Note that the depletion zone at 0 V is a bit noisy, but becomes slightly wider and crispier with a negative gate voltage, and its "growth" in width is towards the drift region, which would have a greater reservoir of charge. At +0.5 V, the depletion zone is still detectable, but is perhaps more easily seen in the (black) curve shown in Figure 10. By +1.0 V, the zone is not detectable either with the eye or in the line profile of the electrical data. These are indications of the turning on of the MOSFET portion of the IGBT. These results may seem surprising, given that this depletion zone disappears at voltages lower than the typically reported operating voltages of around 5 V. It is to be noted however that this paper is only dealing with the MOSFET: higher voltages would likely be required to turn on the bipolar transistor.
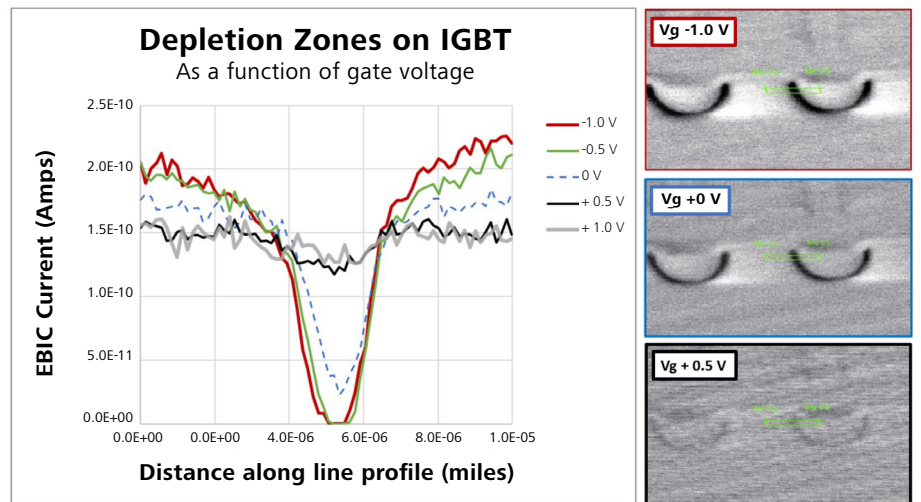

Figure 10 Numerical comparison of the current data taken across line profiles for several gate voltages in the study. The red, blue, and black boxes help to identify which curves are associated with associated EBIC results.
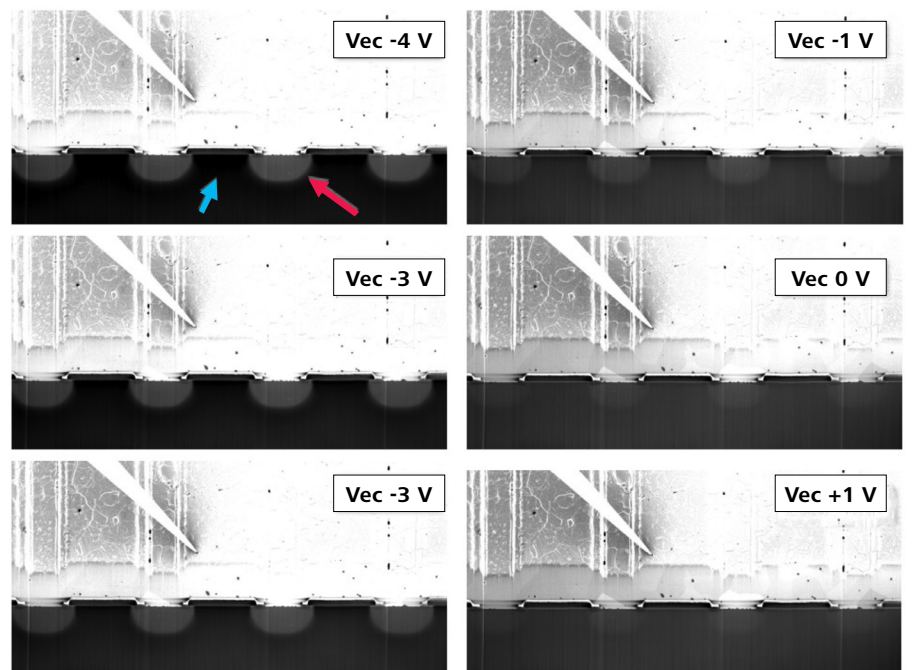

Figure 11 Active voltage contrast images of the device in cross section, examined with various values of Vec. The red arrow highlights the P- body region; the blue arrow highlights the much darker N- drift region. A sampling of the voltages in the experiment is shown here.

D. Active Voltage Contrast

Next, the ability of the exposed surfaces to respond to an AVC [22,23] was explored. A probe was placed on the emitter, which, because of the structure of this device, is also the top surface metal. A second, grounded probe was placed on the surface of the exposed silicon in the N- drift region. SEM images were then taken as the voltage on the emitter was varied across nine different voltages, from -4.0 V to 4.0 V. A sampling of these images is shown in Figure 11. It is important to note that in this context the emitter is directly touching the P-body of the device. It is apparent that at negative voltages, which would reverse-bias the diode between the P-body and N-drift regions, the VC effect becomes stronger. And at forward bias or positive voltages, the contrast between the two largely goes away.

A quantitative exploration of these AVC results is shown in Figure 12. The relative SEM brightness of P- body, and N-drift are compared, along with the cross-section of the metal as a control. The brightness value of 50 pixels within a rectangular area was recorded for each type of material, averaged, and normalized to the brightest feature in the whole set of data. The graph in Figure 12 shows curves for these three materials, and its accompanying micrograph shows blue boxes for the locations the brightness values were averaged on the images. Several observations may be made: First, it is apparent that the metal and P-regions continue to get darker across the range as the voltage becomes more positive. This intuitive result is likely a simple effect of electron affinity of the biased surfaces.
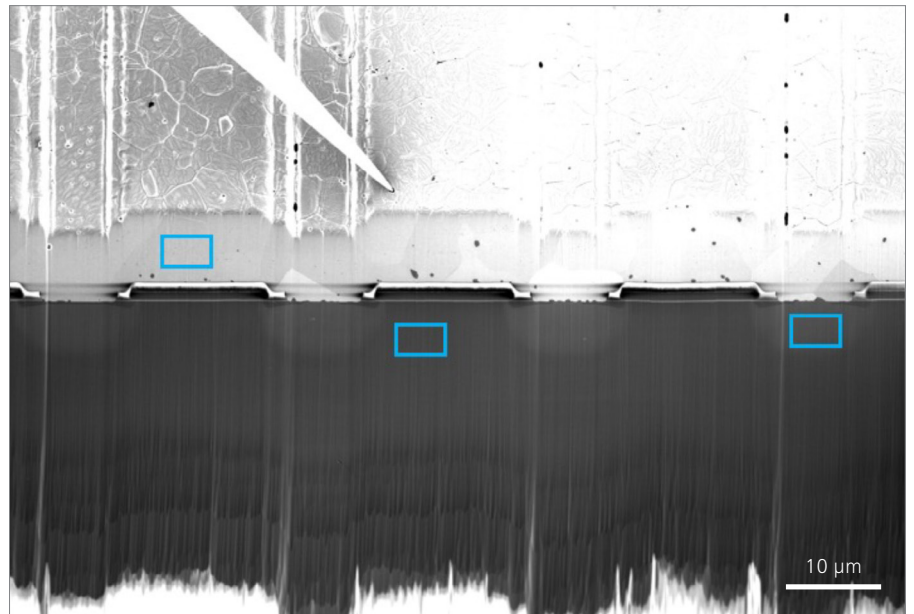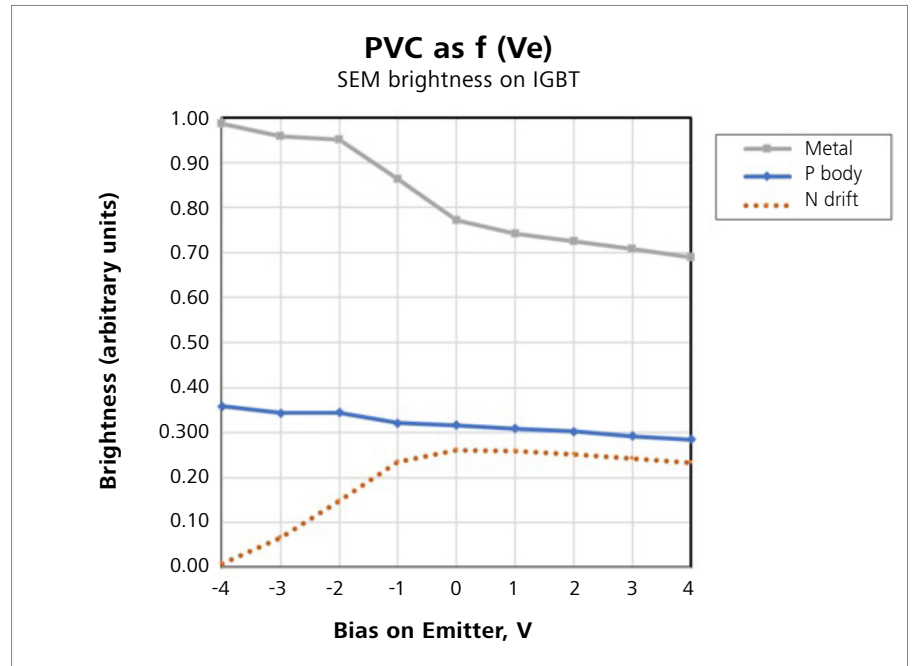
However, the N- region gets brighter, and then proceeds to follow the pattern of the P- material with increasing voltage. As the *p/n* junction is biased, the barrier of the junction is reduced and allowing current to flow.

It is proposed that this work points to the applicability of nanoprobing on junctions as a means to learn about band diagrams. It also shows another expected property of junctions was not adversely affected by the GaFIB milling operation.

Figure 12 *Plot of relative brightness in the SEM image across 50 pixels for each of metal, P-, and N- regions in the AVC study. The blue boxes highlight the areas compared on each of nine different images.*

Conclusions

An experimental FIB wedge shape was milled into an IGBT chip. Through this window, the properties of voltage contrast, unbiased EBIC, EBIC as a function of gate bias, and active voltage contrast were all reported. It was shown that the imaging conditions chosen in the SEM and EBIC system were sensitive enough to simultaneously image both *n/p* and *p/n* junctions, with oppositely oriented electric fields, and therefore opposite EBIC signals. These depletion zones were able to be scrutinized in great detail, easing concerns about amorphization or Ga+ implantation effects from the FIB operation [24, 25]. The burden of proof may have shifted to those who would object to the use of Ga in junction analysis, at least for failure analysis (as opposed to metrology), at least for power devices. These results provide novel insights as to the inner workings of an IGBT device. This wedge-cut also left intact the contact pads on the surface of the chip, enabling the *in situ* observation of device parameters as a function of gate voltage.

These techniques would also be critical for work on rotated wafers, where mechanical cross sections normal to the surface will be difficult. This paper has brought new insights into the workings of the MOSFET portion of the IGBT.

Future Work

These results have strong merit for the power devices examined, devices in which junctions go "deep into the page", or the z dimension of structures is tens of microns long. Further work will examine the suitability such FIB cuts in devices with much smaller features such as finFETs or GAA devices. An additional set of experiments were carried out, attempting to measure the I-V curve of the *p/n* junction while the gate bias was varied. These results are not reported here, but may be published for a future paper after further optimization of the technique.

References

[1] E. M. Findlay, High Efficiency IGBTs through Novel Three-Dimensional Modelling and New Architectures, Cambridge, 2020.

[2] S. Davis, ""Back-to-Basics: Power Semiconductors"," *Power Electronics,* no. July 26, 2012.

[3] S. Linder, "Power Semiconductors, Part One: Basics and applications," *ABB Review,* no. 4/2006.

[4] M. Rahimo, "Power Semiconductors for Power Electronics Applications," in *CAS-PSI Special Course, Power Converters,* Baden, Switzerland, 8 May 2014.

[5] B. Kok, M. Looi and H. Goh, " Insulated Gate Bipolar Transistor Failure Analysis in Overvoltage Condition," in *ICREPQ'12.*

[6] N. Valentine, D. Das and M. M. Pecht, "Failure Mechanisms of Insulated Gate Bipolar Transistors (IGBTs)," in *2015 NREL Photovoltaic Reliability Workshop.*

[7] "Insulated Gate Bipolar Transistor (IGBT) Operation," Electrical A2Z, [Online]. Available: https://electricala2z.com/electronics/insulated-gate-bipolar-transistor-igbt-operation-characteristics/. [Accessed 19 January 2022].

[8] U. Celano, K. Paredis, A. D. L. Humphris, M. Tedaldi, C. O'Sullivan, J. P. Hole and J. Goulden, "An innovative probe microscopy solution for measuring conductivity profiles in 3-dimensions," in *Proceedings Volume 11611, Metrology, Inspection, and Process Control for Semiconductor Manufacturing XXXV,* Online Only, 2021.

[9] U. R. M. Schlapbach, C. von Arx, A. Mukhitdinov and S. Linder, "U. R. M. Schlapbach, C. von Arx, A. Mukhitdinov and S. Linder, "1200V IGBTs operating at 200°C? An investigation on the potentials and design constraints," in *ISPSD,* Jeju Island, Korea, 2007.," in ISPSD, Jeju Island, Korea, 2007.

[10] B. J. Nel and S. Perinpanayagam, "A brief overview of SiC MOSFET failure modes and design reliability," in *The 5th International Conference on Through-life Engineering Services,* 2017.

[11] J. R. Beall and J. L. Jamiter, "EBIC - A Valuable Tool for Semiconductor Evaluation and Failure Analysis," *15th International Reliability Physics Symposium,* pp. 61-69, 1977.

[12] K. Nikawa, "Method and system for testing an interconnection in a semiconductor integrated circuit," *US Patent number 5,804,980.*

[13] A. Rummel, G. Johnson and M. Kemmler, "Low-voltage EBIC investigation of EBIC fails," *IPFA,* 2021.

[14] E. Cole, ""Beam-Based Defect Localization Techniques"," *ISTFA,* vol. Tutorials, 2007.

[15] G. Johnson and A. Rummel, "Use of passive, quantitative EBIC to characterize device turn-on in 7 nm technology," *European Society for Reliability and Electrical Failure Analysis,* 2021.

[16] M. Simon-Najasek, J. Jatzkowsk, C. Große and F. Altmann, "A New Technique for Non-Invasive Short-Localisation in Thin Dielectric Layers by Electron Beam Absorbed Current (EBAC) Imaging," *ISTFA,* 2012.

[17] G. Johnson, J. Saujauddin, T. Rodgers and J. Lee, "Characterization of electronic devices by top-down Electron Beam Induced Current," *IPFA,* pp. pp. 1-5, 2020.

[18] G. Johnson and A. Rummel, "Use of passive, quantitative EBIC to characterize device turn-on in 7 nm technology," *ESREF,* 2021.

[19] V. Viswanathan, G. Johnson, R. Rummel, J. Jokisaari, S. McCracken, S. Costello, A. Robinson, A. Gibson and A. Balfour, "Simple Methods for Evaluating Junctions in IGBTs," in *International Symposium for Testing and Failure Analysis.,* 2022.

[20] H. Stegmann, G. Johnson and A. Rummel, "Characterization of power semiconductor junctions by combining three dimensional FIB-SEM imaging and EBIC," in *CAM workshop,* Halle, Germany, 2023.

[21] G. Johnson, A. Rummel, H. Stegmann and C. Huang, "In-situ measurement of depletion zones in power devices," in *ASMC,* Saratoga Springs, NY, 2023.

[22] Osterreicher, U. Rossberg and S. Eckl, "Active Voltage Contrast and Seebeck Effect Imaging as Complementary Techniques for Localization of Resistive Interconnections," in *ISTFA 2008.*

[23] R. Rosenkranz, ""Failure localization with active and passive voltage contrast in FIB and SEM"," *Journal of Materials Science-materials in Electronics,* 2011.

[24] D. Zudhistira, M. Wei, V. Narang, J. Chin, M. Š. Sharang, K. Novotný, G. Goupil, J. V. Oboňa, A. Rummel, M. Kemmler and S. Kleindiek, "Integration of Probing Capability into Plasma FIB for In-Situ Delayering, Defect Inspection, and EBAC on BEOL Defects of Sub-20nm FinFET Devices," *ISTFA,* 2018.

[25] K. Pandey, K. Paredis, T. Hantschel and e. al., "The impact of focused ion beam induced damage on scanning spreading resistance microscopy measurements," *Sci Rep,* vol. 10, no. 2020, p. 14893.

[26] D. Zudhistira, V. Viswanathan, V. Narang, J. Chin, S. Sharang, K. Novotny and J. V. Oboňa, "Plasma FIB Delayering for Physical Failure Analysis of Sub 20-nm Microprocessor Devices," *ISTFA,* 2017.

Zero Channel Bias Determination of Device Turn-on and the Seebeck Effect in Nanoprobing

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Seeing beyond

Abstract

In prior work, it was demonstrated that information about device turn-on can be obtained in a nanoprobing setup which involves no applied bias across the channel. This was performed on nFET logic devices in 7 nm technology and attributed to the Seebeck effect, or heating from the SEM beam. In this work, the experiments are continued to both nFET and pFET devices and on both 22 nm and 5 nm devices. Further discussion about the opportunities and evidence for Seebeck effect in nanoprobing are discussed.

Introduction

Nanoprobing is an increasingly important part of a physical failure analysis approach to semiconductor yield management. It provides the ability to characterize the full set of transistor properties of individual devices. Given the presence of an electron beam, and probes capable of measuring currents or voltages, it also opens a full suite of techniques for defect localization and device characterization, including EBIC, EBAC, EBIV, and EBIRCH [1-8].

As semiconductor technology advances into ever smaller technology nodes, so does the concern that failure analysis techniques do not damage or over-stress these smaller components. This concern relates not only to beam energy applied during an analysis technique but also to the currents and voltages applied directly to a sample. Hence, there will always be a need for new analytical methods to look for opens or shorts, analyze junctions, or to detect which fin may be active in a device. Furthermore, as new technologies introduce device architectures that are more complex, there may be a need to examine features which are not as easily accessible by probe tips. It is in the scope of these concerns that this paper derives merit.

As the Seebeck Effect is a major theme of this paper, it would be useful to introduce the concept here, and offer typical values for common materials used in electronics. When two dissimilar materials, of Seebeck coefficients Q_1 and Q_2, are brought into contact, and the junction is heated, an electromotive force or seebeck voltage is generated [9-11]. This voltage is given by the equation, $\Delta V = (Q_1 - Q_2) \Delta T$.

Typical values for materials used in semiconductor devices and/or the testing of them are shown in Table 1. It should be noted that nanoprobing typically involves the use of tungsten probe tips, and these tips are typically in direct contact with copper, cobalt, or tungsten features on the devices.

Seebeck coefficients (µV/K)

Material	Value	Source
Tungsten	7.5	[9]
Copper	6.5	[9]
Cobalt	-30.8	[10]
SiC	-20 to -108	[11]
Si	440	[9]

Table 1 *Seebeck coefficients of materials often encountered in nanoprobing*

Prior Work

In a previous paper [4], it was shown that it is possible to obtain information about device turn-on in a 7 nm logic transistor even with no channel bias, or zero V_{ds}, applied to the device. The experimental setup is described in Figure 1. A chip containing an SRAM is delayered to contact level by mechanical polishing. Then one side of the device (arbitrarily referred to as "drain" in this paper") is grounded with a nanoprobe probe tip. From the other side, a tip is placed which is the EBIC sensing needle, and also grounded. The gate contact meanwhile may have any voltage applied to it. The only EBIC signals measured in this setup are those from the bottom probe.

The results from that earlier work are reported in Figure 2. Again, it is important to note that the sensing contact is at the bottom in the image. At a gate voltage of 0.0 V, the only signal in the field of view is on the source side. This result is not unlike a typical EBAC result for any via chain or signal contact. In this experimental setup, black values indicate currents which represent a net loss of electrons from the probe. Now, as the gate voltage is increased, from 0.0 V to 0.4 V, we can gradually see an image form on the other side of the gate, albeit with opposite contrast, indicating a net gain of electrons.
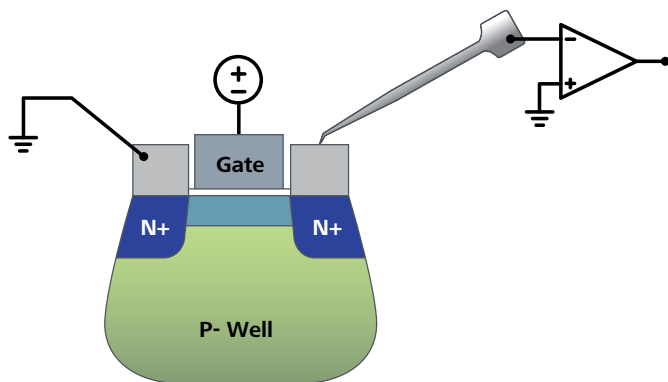
Figure 1 Diagram describing the experiments undertaken. A transistor is grounded on one side. Various voltages are applied to the gate, and then the current is measured at the other contact, which is also grounded.

The prior work attributed the appearance of a spot of opposite contrast after gate turn-on to the Seebeck effect at the far contact providing a potential that is picked up in the system. In that study, two separate examples of similar devices confirmed this effect. A careful examination of the images Figure 2 show that the primary signal occurs rather uniformly across the bulk of the contact, and is therefore is unlikely to be related to the electron beam "wrapping around" the edges of the contact, as might be expected if a true EBIC effect from beam interaction with buried *p/n* junctions were the dominant or only phenomenon at play. The turn-on was detected with zero bias applied across the channel.

Procedure

This work used two different commercially available chips, one from a 22 nm technology node, and one from 5 nm. The chips were polished to contact level by mechanical means. They were imaged in a GeminiSEM 300 FE-SEM equipped with a PS8e Prober Shuttle. EBIC scans were undertaken according to the setup of Figure 1, with source and drain contacts grounded, measuring only the current from one side, while the voltage was varied on the gate. These experiments were undertaken with the hypothesis that examining both nMOS and pMOS devices could demonstrate that Seebeck effects were at play in the phenomenon discovered by the prior paper.

Results

22 nm

The field of view chosen for the first experiment is shown in Figure 3. It is a typical 22 nm SRAM, with the actual nMOS and pMOS devices which underwent probing being displayed at higher magnifications in Figure 4. As the gate voltage was increased from 0.0 V to 1.2 V, a series of EBIC images were collected, while both the source and drain sides of the transistor were grounded. The acceleration potential was 0.5 kV and the scan time was 3.4 minutes.
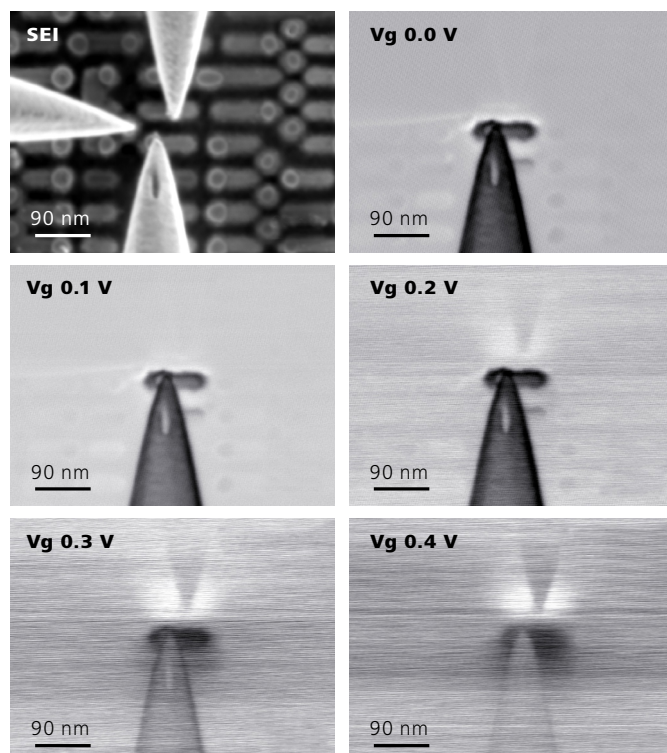

Figure 2 Previous work [4] demonstrating device turn on in an nMOS 7 nm logic device. Note that the signal is uniformly strong across the surface of the contact itself. This is incompatible with the distribution of EBIC signal expected if the phenomenon were instead due to the electrons "bleeding around" the edge into the underlying silicon.
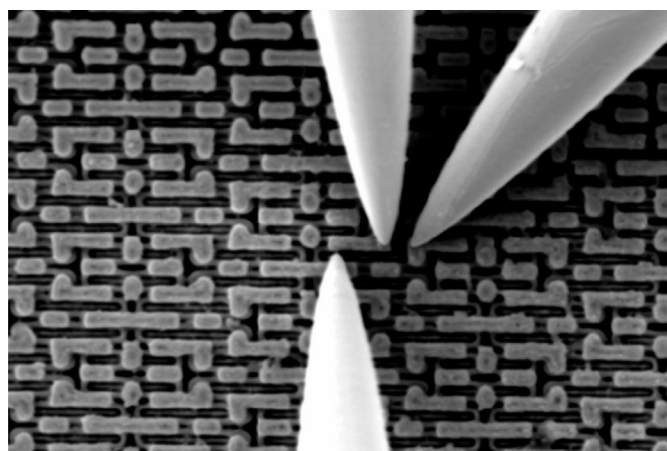

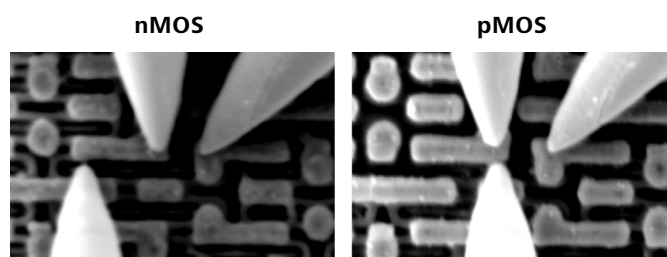Figure 3 Low mag view of 22 nm SRAM examined in this study.

Figure 4 SEM view of the devices probed in the 22 nm sample.

Figure 6 New EBIC results comparing device-on results for nMOS vs pMOS devices on a 22 nm SRAM.

Figure 7 Schematic overlay on top of EBIC signal. The two probe tips are shown in white, the contacts in yellow, and the approximate placement of fins are shown as well.
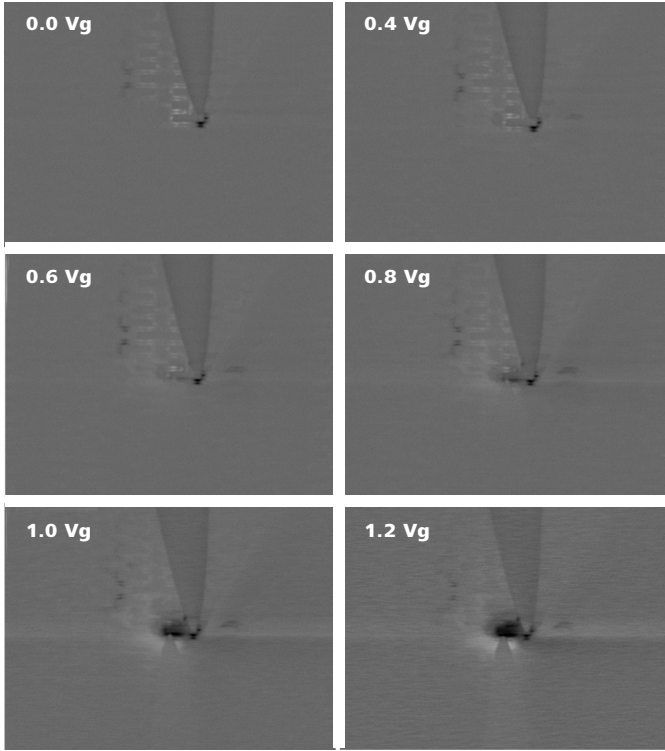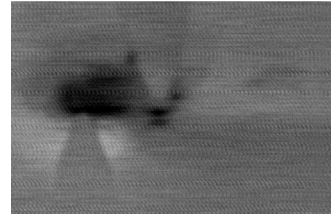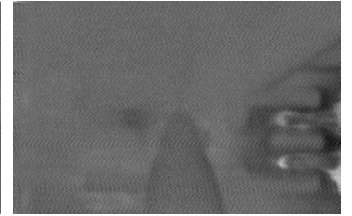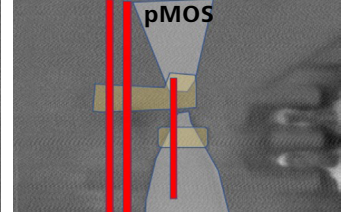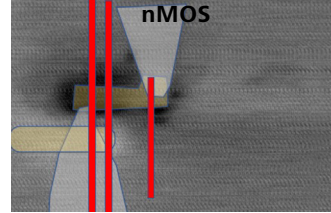
Figure 5 EBIC results on 22 nm nMOS device for a series of experiments with both source and drain grounded, but an increasingly higher gate voltage, from 0.0 V, 0.4 V, 0.6 V, 0.8 V, 1.0 V, and 1.2 V.

5 nm

The same sort of experiment was now repeated on a 5 nm SRAM array. The field of view for the 5 nm device is depicted in Figure 8. To provide some assurance that the devices were not harmed by the delayering process, a transistor family of curves were measured, and are shown in Figure 9. Now, the same experiments were repeated. The endpoints of these two experiments are shown in Figure 10. The nMOS again shows black and white signals, with the pMOS essentially showing noise.
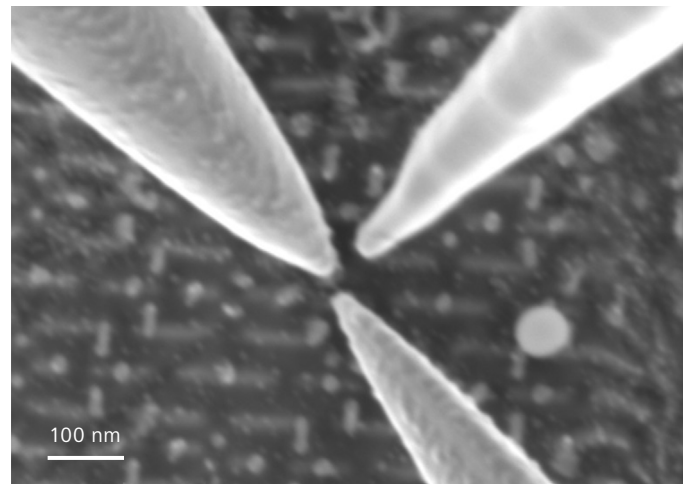
The series of EBIC images are displayed in Figure 5. At low voltages, there is a very slight, black, EBIC/EBAC signal just outside the contact. This may be due to the electron beam wrapping around the contact and interacting, directly, or with capacitive coupling, with the p/n junction underneath. However, as the device is turned on, we eventually see a crisp signal of black (loss of electrons) at the measured tip, with a white signal (gain of electrons) showing up at the far tip. The procedure was repeated in both directions (switching active probe tip) for the nMOS, and gave similar results, but are not shown here.

Next the experiment was repeated for the pMOS device, with the results of each type display at higher-resolution in Figure 6. As expected from the prior work, the nMOS shows a pair of very strong black/white signals, concentrated on the contact itself, while the pMOS hardly shows any signal at all. This was not our predicted hypothesis. Figure 7 is offered as a courtesy to show how fins (red) would correspond to the structure in question, with a yellow overlay for the contact. There is some effect on the edges of the measured contact (upper, black), but a significant one in the contact itself. Meanwhile the further contact (Figure 6, left, bottom) reveals a much stronger signal at the contact, per se.

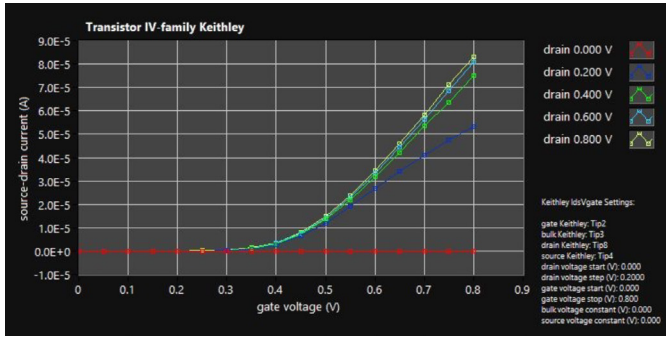Figure 8 Field of view for the measurements on 5 nm device.

Figure 9 *Transistor family of curves for 5 nm nMOS, providing reassurance of quality and integrity of devices upon delayering.*

Summary

Across a careful examination of three technology nodes (22 nm, 5 nm, and the prior work on 7 nm) these works have confirmed that for nMOS devices, some indication of device turn-on may be provided even in a scenario where there is zero channel bias. Some native effect is detected across the channel when the device is turned on. Again, this phenomenon being measured on three technology nodes provides some assurances it's a property of the physics of semiconductor devices and not some consequence of a strange design or damage in delayering of one chip. Meanwhile, in pMOS, there is no practical measurement of this effect, as demonstrated on both 5 nm and 22 nm devices. (The prior 7 nm work was only on nMOS.)

The EBIC hypothesis

If this effect – one of black/white spots across a zero-bias channel in EBIC measurements – were merely due to the EBIC effect of *p/n* junctions, there should be at least two consequences. One, the effect should be stronger around the edge of devices, and not as strong effect across the bulk of the contact itself. This is because it is well-known that there will be greater beam penetration through oxides than through metals such as tungsten or cobalt. Thus, the signal should be stronger just outside the contact than over it. Secondly, the two types of contact, nMOS and pMOS, would therefore have *p/n* junctions underneath them of opposite polarity. Any effects due to fields or work function should simply change the direction of the effect. In fact, this should mean a swap in color polarity between the two effects. This was not observed: the effect turned off on pMOS. Similarly, it could be argued that if this were due to an EBIC effect, (or similarly, due to a PVC effect), that the two contacts themselves would have the same polarity in the nMOS. Instead, they are opposite in contrast.
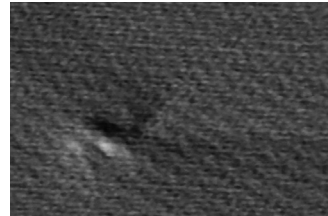
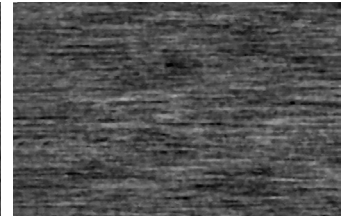**nMOS, +0.8 Vg**   **pMOS, -0.8 Vg**

Figure 10 *Results of EBIC experiments in 5 nm, for both nMOS and pMOS, at the higher voltages. Again, source and drain are grounded during these runs.*

The Seebeck hypothesis

Certain aspects of these results are compatible with a Seebeck explanation alone. First, as said before, the signal is often uniformly strong across the area of the contact itself, which would be not only due to the place where the Seebeck junction exists, but also due the fact that denser metals are more likely to heat up than oxides. Secondly, the fact that the near and far contacts have opposite contrasts fits well with the way the vector contacts are arranged. The nMOS results are easily explained by the Seebeck effect. Let's check again whether Seebeck effects were a credible phenomenon in electron-beam based nanoprobing.

A defense of Seebeck

Perhaps it would be a useful diversion to provide additional evidence that Seebeck effects can be detected at all by traditional EBIC/EBIRCH measurements in nanoprobing. The first example is shown from prior work where EBIRCH analyses are possible in BEOL systems containing no *p/n* junctions whatsoever. In this example the shorts contain a short between copper and liner material, thus providing an interface that can be activated by the temperature effects from the beam and the Seebeck effect. One such example is Figure 11, from [5]. In this work, EBIRCH isolated a short between two copper lines joined by tantalum.
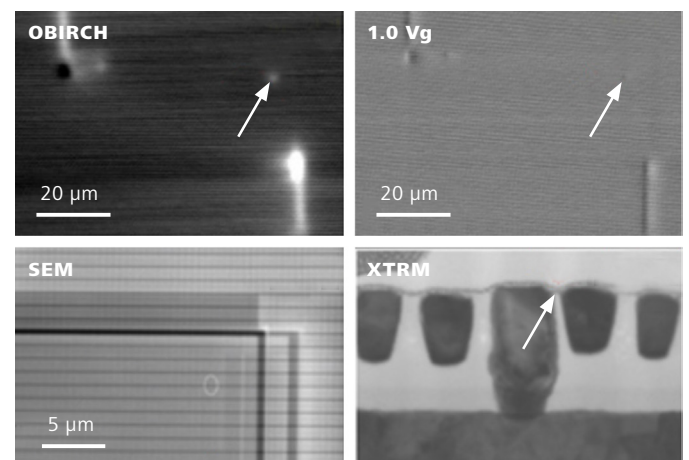

Figure 11 *Example of the use of EBIRCH to localize a short in a BEOL via chain. No p/n junctions are involved, and the cross section showed the short involved a liner interface, which would have introduced a material (Ta) with very different Seebeck coefficient from Cu. From [5]*

Additional evidence that Seebeck effects readily happen in nanoprobing is shown in examples where the tungsten probe tip is in direct contact with material and is in the field of view during imaging. One such example is shown in Figure 12, which represents an attempt to perform EBIRCH analysis on a BEOL test structure, which does not even contain any *p/n* junctions at all. The red arrows point to the places where a tungsten needle is in contact with a test pad, and there is no effect in these places. Tungsten and copper have very similar Seebeck coefficients, and thus no Seebeck effect is noted. (Meanwhile, a slight effect is actually seen at the edge of the pads, and this may actually be due to a Seebeck effect between the linear of the test pads and the test pads themselves).
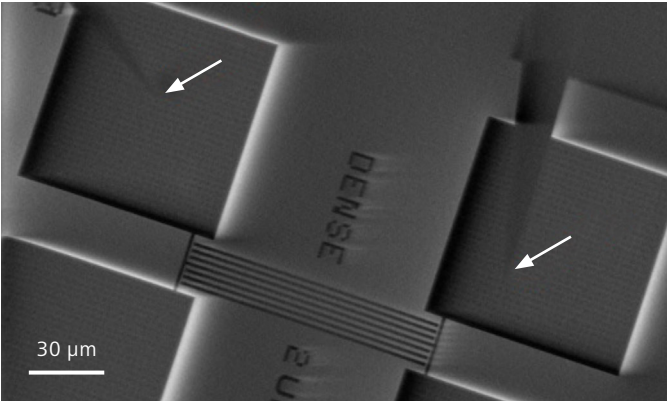

Figure 12 *Example of EBIRCH analysis at 30 kV on a BEOL test structure (containing no* p/n *junctions). Note that there is no signal at the interface between copper test pads and the probe tips (red arrows). Johnson, unpublished work.*

In contrast, in the cases of nanoprobing experiments which where a tungsten probe tip is placed directly on silicon, typically there is an extremely large, unuseful, and distracting signal. Such analyses are typically carried out without the needle in the field of view. Two such examples are provided in Figure 13.
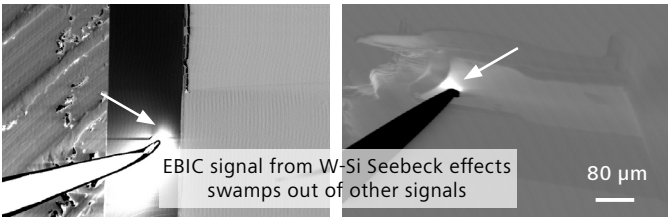

EBIC on SiC x-section, 5.0 kV   EBIC on IGBT (Si) lamella, 5.0 kV

Figure 13 *Examples of the typical EBIC/EBIRCH effects observed when a tungsten probe tip touches bare silicon. Left, lamella prepared from an IGBT device. Right, cleaved cross section of an SiC MOSFET. The signal is swamped out at the point where the tungsten needle hits silicon. It is proposed that the Seebeck effect of this interface swamps out any EBIC signals within the device cross section.*

One is a SiC MOSFET, and the other is a lamella of an IGBT sample (with silicon bulk). Furthermore, additional papers have pointed to Seebeck or beam heating as a mechanism in electron beam analyses of samples [12-14].

Models for Seebeck effects
nMOS
The nMOS case is relatively straightforward and is depicted as back-to-back intermetallic junctions in Figure 14. The Seebeck effect is in play, serially, at each interface. Hence negative or positive deviations from the baseline are registered in the analysis software. Across three technology nodes, white and black spots were seen at the far and near contacts, respectively, in EBIC. It is understood that the Seebeck effect describes a voltage, but there are some treatments of it that speak of it, perhaps intuitively, as effects on a 2-dimensional electron gas.
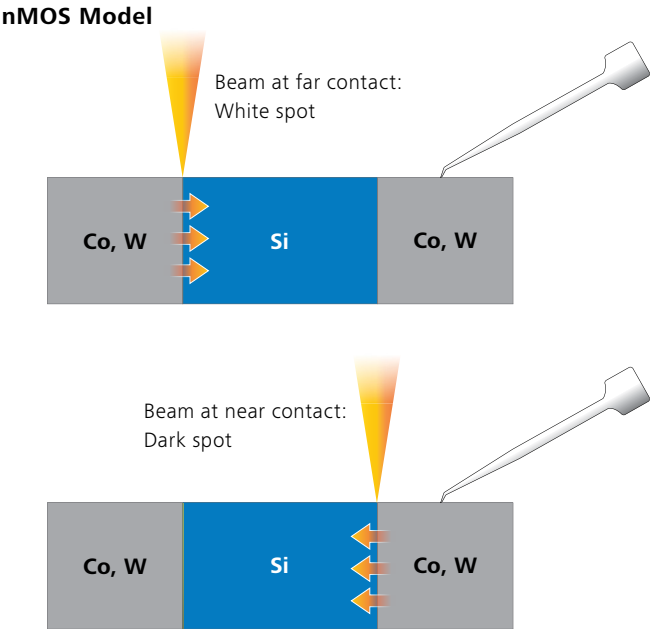
nMOS Model

Figure 14 *Model for nMOS case, considered with the gate open. As beam hits the W/Si (or Co/Si) interface at the far contact, the Seebeck electromotive force helps drive a current into the probe, and reported as a white spot. As the beam hits the near spot, the Seebeck effect has the opposite effect as seen from the probe tip and is reported as a dark spot.*

Doping	n-type	p-type	Source
Doped 10^{15}/cm^3	-1400	1500	[15]
Doped 10^{19}/cm^3	-450	550	[15]
Nanowires	-170	162	[16]

Table 2 *Seebeck coefficients of silicon under various doping conditions.*

pMOS

The pMOS case is more difficult as one will have to explain why there a greatly reduced tendency to see these effects. One possible explanation is that the Seebeck coefficients for n-type and p-type silicon are similar in magnitude but opposite in sign, according to the values in Table 2. If this were the only driver, this would simply mean a reversal of the signs on the current, or a switching of the black and white spots. Frankly, this was the hypothesized result, but it did not take place.

However, a mechanism becomes more clear when one considers that the pMOS contact is sitting on top of a *p/n* junction, where the built-in potential provides a sink for electrons. (Alternatively, one might think of it in terms of the orientation of the field at this junction). Thus, any effects taking place as these interfaces might not be detected at the probe tip. That this might not cause a problem for the N$^+$/PW junction underneath the nMOS contact is left as an exercise for the reader.
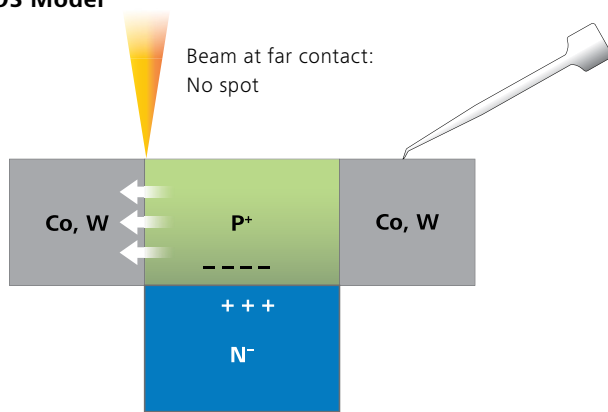
pMOS Model

Figure 15 *Model for pMOS case. Even if Seebeck effects of similar magnitude exist, any flux of electrons will find a sink in the positively charged N-well, due to the built-in potential of the junction.*

Conclusions

This work has demonstrated that transistor turn-on may be detected and quantified using a technique that applies zero bias across the channel in nMOS devices. It was confirmed by analyzing devices on chips from three different technology nodes. Painstaking work has demonstrated that Seebeck effects can and do happen in typical nanoprobing conditions, from BEOL structures containing no *p/n* junctions at all, to tungsten probe tips touching silicon.

The implications of this work will have a variety of applications, from providing ideas for the measurement of extremely delicate devices, to ideas for the measurement of complex systems where some circuit elements may be easier to reach with a SEM beam than a needle, to providing nanoprobe users some guidance in the interpretation of spurious, unuseful signals in an EBIC analysis. Further consideration of the mechanism provides further evidence that the Seebeck effect is at play in nanoprobing based localization techniques and should be considered in the interpretation of any such measurement.

References

[1] J. R. Beall and J. L. Jamiter, "EBIC - A Valuable Tool for Semiconductor Evaluation and Failure Analysis," *15th International Reliability Physics Symposium,* pp. 61-69, 1977.

[2] E. Cole, ""Beam-Based Defect Localization Techniques"," *ISTFA,* vol. Tutorials, 2007.

[3] D. Dahanayaka, D. Bader, D. Prevost, M. Coster, E. Mccullen, M. Masters and K. Stevens, ""Intra-Device Defect Localization through EBIC/EBAC Combined with Electrical Nano-Probing for FinFET Devices Composed of Multiple Sub-Elements"," *ISTFA,* 2016.

[4] G. Johnson and R. A., "Use of passive, quantitative EBIC to characterize device turn-on in 7 nm technology," *ESREF,* 2021.

[5] G. Johnson, C. D'Aleo, Z. Xu, U. Kwon, H. Berman, Y. Feng, S. Darling, B. Yates, Y. Wang, M. Kagerer and R. Newton, "Electron Beam Induced Resistance Change for Device Characterization and Defect Localization," *ISTFA,* 2016.

[6] G. Johnson, A. Rummel, M. Kemmler, T. Lundquist and B. Niu, "Probing SRAM Signals for Yield Management," *IPFA,* 2019.

[7] G. Johnson, J. Saujauddin, T. Rodgers and J. Lee, "Characterization of electronic devices by top-down Electron Beam Induced Current," *IPFA,* pp. pp. 1-5, 2020.

[8] K. Nikawa, "Method and system for testing an interconnection in a semiconductor integrated circuit," *US Patent number 5,804,980.*

[9] C. J. M. Lasance, "The Seebeck Coefficient," 1 November 2006. [Online]. Available: https://www.electronics-cooling.com/2006/11/the-seebeck-coefficient/. [Accessed 26 August 2022].

[10] O. R. Onvural, "Thermoelectric devices with controlled current flow and related methods". Patent WO2006033875A2, 2005.

[11] N. A. M. A. R. R. L. Abu-Ageel, "The Seebeck coefficient of monocrystalline α-SiC and polycrystalline β-SiC measured at 300–533 K," *Semiconductor Science and Technology,* vol. 15, pp. 32-33, 2000.

[12] Osterreicher, U. Rossberg and S. Eckl, "Active Voltage Contrast and Seebeck Effect Imaging as Complementary Techniques for Localization of Resistive Interconnections," in *ISTFA 2008.*

[13] D. Bouscaud, P. Pesci, S. Berveiller and E. Patoor, "Estimation of the electron beam-induced specimen heating and the emitted X-rays spatial resolution by Kossel microdiffraction in a scanning electron microscope," *Ultramicroscopy,* pp. 115-119, 2012.

[14] H. Choi, S. Heo, H. Hong, S. Yang, Y. Han, Y. Cho, S. Won and T. Park, "High Resolution Short Defect Localization in Advanced FinFET Device Using EBAC and EBIRCh," in *IPFA,* Chengdu, China, 2017.

[15] M. Wagner, "Simulation of Thermoelectric Devices (dissertation)," 2007.

[16] Y. Hyun, Y. Park, W. Choi, J. Kim, T. Zyung and M. Jang, "Evaluation of Seebeck coefficients in n- and p-type silicon nanowires fabricated by complementary metal–oxide–semiconductor technology," *Nanotechnology,* vol. 23, no. 40, 2012.

[17] B. J. Nel and S. Perinpanayagam, "A brief overview of SiC MOSFET failure modes and design reliability," in *The 5th International Conference on Through-life Engineering Services,* 2017.

[18] S. Linder, "Power Semiconductors, Part One: Basics and applications," *ABB Review,* no. 4/2006.

[19] H. Zhou, P. Kropelniciki, J. M. Tsai and C. Lee, "Study of the Thermoelectric Properties of Heavily Doped Poly-Si in High Temperature," *Procedia Engineering,* vol. 94, no. https://doi.org/10.1016/j.proeng.2013.10.011, pp. 18-24, 2014.

EBIRCH Localization for Low-current Soft Fails

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Seeing beyond

Abstract

An experimental study was undertaken to determine the minimum level of leakage or shorting current could be detected by EBIRCH. A 22 nm SRAM array was overstressed with aseries gradually increasing bias, followed by EBIRCH scanswith 1 V applied bias and 2 kV SEM imaging, until fins were observed. The result was that with only 12 nA of shorting current, the fins of a pulldown device could be imaged by EBIRCH. Higher stresses created an ohmic short, and careful consideration of experiments with current direction provide additional evidence that EBIRCH is largely a temperature driven,or Seebeck effect.

Introduction

The definition of "soft failures" may vary from company to company, or even team to team, but generally includes cases where there is a highly resistive short across a dielectric, which may only marginally affect device performance [1]. The term "soft error", meanwhile, has typically been applied to one-time radiation events [2], but even then, a variety of leakages have been shown to have effects on true soft errors [3].

Soft failures, by virtue of being highly resistive, are therefore extremely challenging for the optimization of devices. EBIRCH (Electron Beam Induced Resistance CHange) has been shown to be a powerful technique for device characterization and defect localization [4, 5]. EBIRCH involves applying a voltage across a circuit, typically between two nanoprobes, and determining the change in resistance or impedance across the device [6]. This is depicted schematically in Figure 1.

Preliminary Results and Motivation

A 22 nm SRAM was delayered to the contact level by use of mechanical polishing. An intentional overstress was applied between gate and source of a pulldown device. Then the sample was analyzed using a PS8 nanoprobing system provided by Kleindiek Nanotechnik in a ZEISS GeminiSEM 300 electron microscope. The resulting image is displayed in Figure 2. The left image is an overlay of the SEM image, with a color-coded display of the EBIRCH response atop. One can see a distinct spot in the expected location of one of the fins. The right image displays a quantitative mapping of the EBIRCH signal. The relative currents show an increase from a 280 nA background signal (no beam simulation on the defect) to 480 nA over the defect. These values are not calibrated but show a very high level of current. The next experiment was to determine just how low of a current could be detected with an EBIRCH analysis.
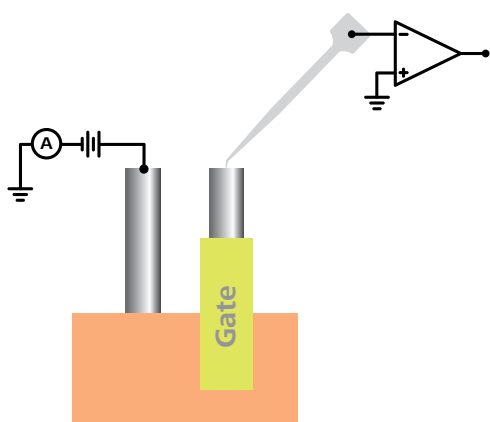

Figure 1 Pictorial view of EBIRCH setup, consisting of two probes, a voltage source, and a means to monitor current. Pictured here is possible probing arrangement in an SRAM.

100 nm

Figure 2 EBIRCH result for SRAM cell taken to 3 V of stress between source and gate, without compliance. Left image is SEM + EBIRCH overlay; right is quantitative analysis. This analysis showed a doubling of the current across the device, from 280 nA to 480 nA, due to beam stimulation.

Procedure and Results

In order to estimate the lowest possible leakage current that could be detected, an experiment of successively higher stresses was undertaken. First, a new device within the same array was chosen, and the baseline current was determined, by applying a voltage up to 1.5 V with a Keithley 4200A SCS source-meter unit. Then, a series of voltage stresses nominally up to 2.5 V were applied, starting with 1 µA, then 2 µA, 3 µA, 4 µA, 5 µA, 6 µA, 8 µA, 10 µA, and 20 µA. The results are shown in Figure 3. One can see that the maximum currents reach no higher than the stated compliance, and the maximum voltage actually decreases during the run. In order to prevent it from going higher than the specified current for the "1 µA" curve, the device was stressed up to 2.7 V before hitting the compliance current. Meanwhile, the 2 µA, 3 µA, 4 µA, 5 µA, 6 µA, 8 µA, and 10 µA curves almost (or nearly) lie on top of each other. For the 20 µA curve, there is a significant change to the shape of the curve, hinting at some alteration of the device.

Figure 4 Current-voltage curves between source and gate for each successive stress in the experiment. Nine successive stresses applied. The current ultimately increased 10x. The bold lines at top and bottom of plot represent pre-stress and post-20 µA stress, respectively.
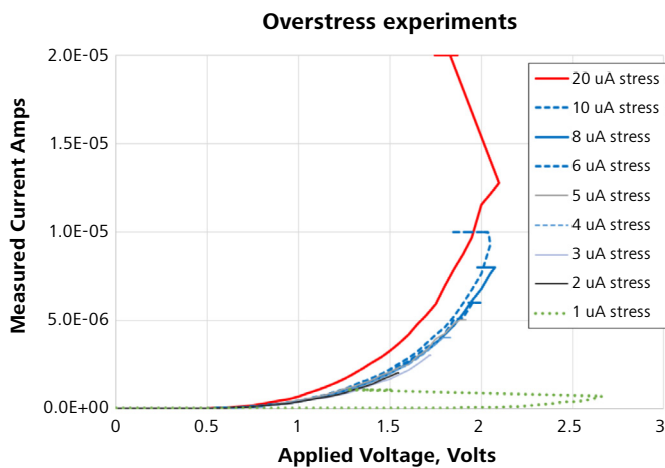

Figure 3 Typical voltages and currents recorded during the overstress experiments. Voltage applied between source and gate of the same pulldown device of a delayered 22 nm SRAM. The 1 µA stress resulted in the device reaching 2.7 V. The rest of the stresses resulted in very similar curves, each ending at the nominal current. The applied voltages decrease as a result of the compliance function.

Next, after each run, a corresponding I-V measurement was recorded between source and drain. These results are displayed in Figure 4. A total of ten curves are displayed, starting with the baseline (purple dotted line), increasing up to the maximum current of the experiment (thick red line). The currents tended to follow a steady increase, with the exception of an unexpected increase after the 3 µA run (sky-blue, or second-highest curve). It should also be noted that all of the I-V curves follow a shape with gradually increasing slope: no straight lines. This is an indication that we have no ohmic conduction, and therefore no metallic bridges creating shorts.
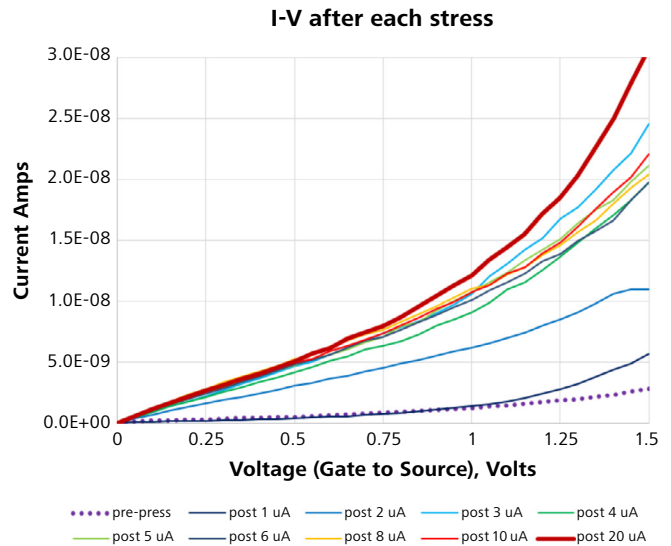
EBIRCH scans were performed with one volt applied bias, and 2 kV SEM imaging across various steps in the experiment. A full set of data and experimental summary are shown in Table 1. The currents steadily, albeit non-monotonically, increase as the stress is increased, at both 1.0 V and 1.5 V. EBIRCH scans were performed after several of the runs, as noted in the table. After 1 µA, 2 µA, 3 µA, and 4 µA, EBIRCH data was simply noise. For the next few increases in stress voltage, EBIRCH was not performed, since no increase in current was observed. Then, with the substantial increase in current after 20 µA stressing, EBIRCH results were performed again.

	Current, Source to Gate, nA		
Operation	**@ 1.0V**	**@ 1.5 V**	**Result**
pre-stress	1.3	2.8	N/A
post 1 uA	1.4	5.7	EBIRCH: noisy pattern
post 2 uA	6.2	11.0	EBIRCH: noisy pattern
post 3 uA	10.6	24.5	EBIRCH: noisy pattern
post 4 uA	9.1	19.7	EBIRCH: noisy pattern
post 5 uA	10.7	21.1	N/A
post 6 uA	10.1	19.7	N/A
post 8 uA	11.0	20.4	N/A
post 10 uA	10.7	22.0	N/A
post 20 uA	**12.1**	**30.7**	**EBIRCH: noisy pattern**

Table 1 Summary of electrical and EBIRCH results for the experiment. N/A means it was not deemed necessary to perform an analysis because there was no change in I/V.

A visual depiction of the results is shown in Figure 5. The results of the first three tests scans are not useful, as they pick up noise or the probes themselves. At 20 µA, however, we have a very nice presentation of the two fins, which would be present in the nFET of a pulldown device. EBIRCH has localized a soft failure with one volt of applied bias, and a leakage of around 12 nA. Figure 6 provides an overlay of the spots onto the SEM image taken at the same time.

The nanoprobing system's Advanced Probing Tool (APT) software was used to plot the current across the devices. These are portrayed in Figure 7. While the values are not calibrated, the currents vary from about 33 nA to 35 nA, indicating that the current values are of the same order of magnitude as those recorded during bench testing, and the EBIRCH analysis picked up a mere 10% increase in the baseline current.
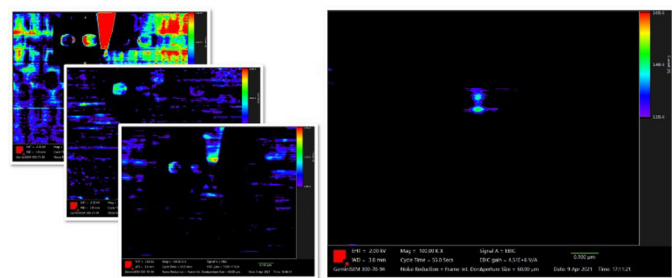
Higher Voltage Stress

The cell was then put through higher stress regimes, as shown in Figure 8. Samples were taken through stress experiments with compliances set at 30 µA, 50 µA, 100 µA, and 200 µA, respectively. The left side of Figure 8 shows that voltages were stopped before 2 V in all cases. The right side shows the current measurement after voltage stress. The I-V curve is essentially linear in the rightmost case, indicating an ohmic short. Yet in all cases, the current running across the short is less than 30 nA @1 V for the highest cell.

An EBIRCH analysis at a beam voltage of 2 kV and 1 V applied bias was run after each of the curves generated in Figure 9. Also depicted in each cell are the maximum curve measured in a line scan across the EBIRCH spot, increasing from 78 nA to 130 nA maximum current. As higher stresses are carried out, a solitary fin provides the more dominant signal, indicating one fin is now contributing most of the leakage current.

Figure 5 *EBIRCH results for 1 µA, 2 µA, 3 µA, and 20 µA overstresses. The lower stress results are full of noise; the analysis after the higher stress highlights the fins of the device.*
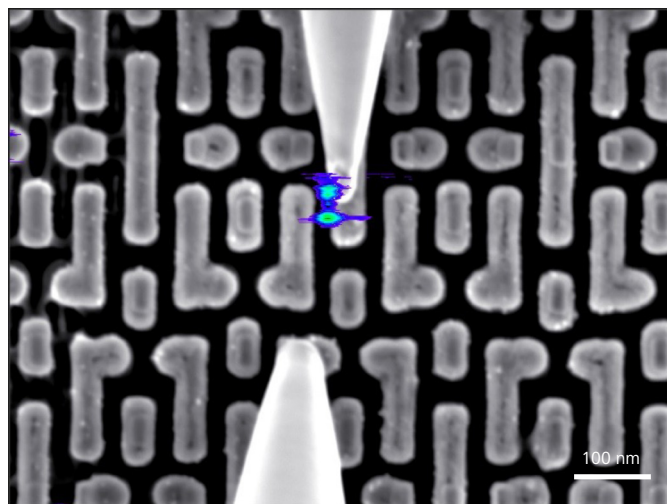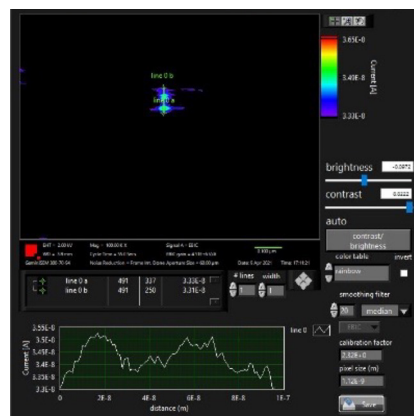

Figure 7 *Quantitative measurement of the EBIRCH response from 20 µA overstress. Note that the absolute value is not calibrated, but there is a 2.5 nA increase in current upon beam stimulation.*

Figure 6 *SEM + EBIRCH overlay after 20 µA stress, nicely highlighting the two fins of the pulldown device.*
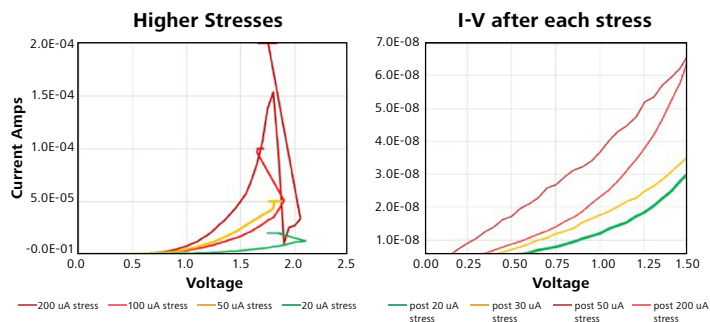

Figure 8 *Stress curves at subsequently higher compliance settings, and a measurement of the current up to 1.5 V after the stress. The highest stress, 200 µA, eventually led to an ohmic short.*
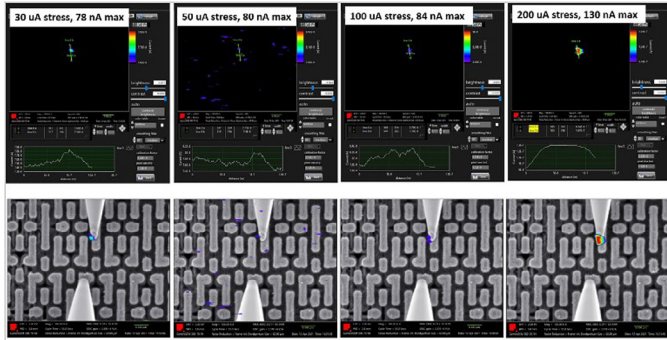
Figure 9 EBIRCH analyses for 30 µA, 50 µA, 100 µA, and 200 µA stress experiments. Top row is quantitative analysis, bottom row contains the SEM overlay of the EBIRCH spot. One fin is stronger and is highlighted in these higher stress experiments. Note also max I increased.
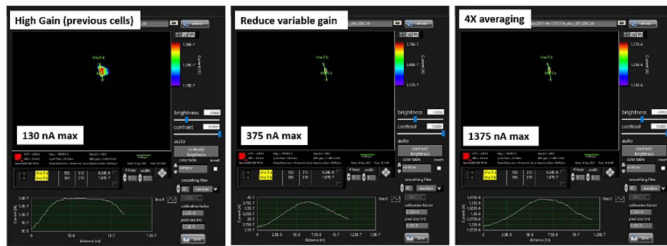

Figure 10 Additional scans post 200 µA with various analysis conditions. The increases remind that EBIRCH is a measure of alteration by the beam, not the raw current.

Figure 11 Experiments varying the probing conditions. Left: Bias, EBIRCH on different probes; Middle: Bias & measure same probes. Right: Lift the ground probe.

Figure 12 Explanation of the arrangement for EBIRCH experiments with "bias applied far" and "bias applied near". The EBIRCH technique can be likened to an ammeter. The two colors of the conduction path highlight that there are dissimilar materials in the conduction path. An electron beam scans from above. The effect of beam heating, according to the Seebeck effect, provides a voltage boost across the interface.

Analysis Conditions

In the previous experiments, the maximum current of the EBIRCH analysis was on the order of magnitude of the current across the channel, if somewhat lower. It would be important to note that these currents from EBIRCH are a measure of the response to the beam, per se, and thus can change depending on how the technique is carried out. This effect is demonstrated in Figure 10. The "regular" or default conditions were run (this is actually the same analysis as the sample on the right of Figure 9). Next the variable gain in the AC portion of the measurement was reduced. Then 4X averaging in the SEM beam was applied. In each case, the current increased.

Probing Arrangement

Finally, a comparison was made to evaluate the effect of various probing arrangements on the analysis and are shown in Figure 11. The left image displays the results from an EBIRCH scan with the same conditions as all the previous ones, with the voltage applying probe being different from the EBIRCH analysis (and ground) probe. Here we see a "white" dot and the line scan reports an increase in current. Then, for the analysis displayed in the middle image, the EBIRCH measurement and voltage applied probe were made to be the same.
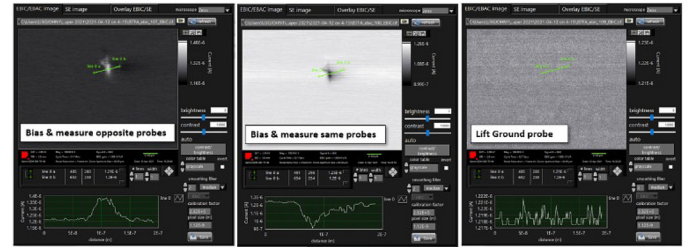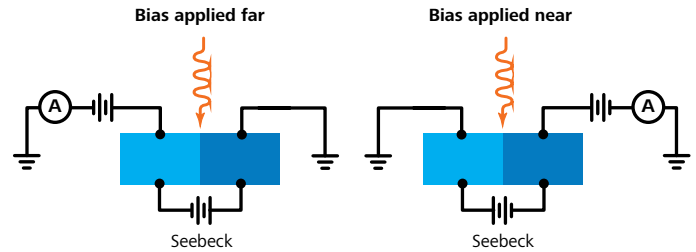
In this case, the results are essentially the same, although inverted in current levels (and therefore contrast). As a visual aid, this arrangement is described pictorially in Figure 12. The EBIRCH measurement can essentially be viewed as a current measurement, and thus is portrayed, if overly simply, as an ammeter. This provides a reminder of the directionality of the contrast and will be explored in greater detail in the next section. Thirdly, the ground probe was lifted, and we have a noisy plot. This provides an indication that the current was through the device and not the well itself.

Discussion of Seebeck Effect

It will now be useful to consider what implications one may draw about the nature of the EBIRCH effect. First of all, it's been established that the defect is an ohmic short, both in terms of the straight line in the current-voltage plot (red curve, right side of Figure 8) during the post-stress evaluation. And secondly, the baseline current is the same during the actual EBIRCH analysis, regardless of which end of the current path the bias is applied to (first two plots in Figure 11). The current profiles of the two analyses are compared as line scans across the defect in Figure 13. One can see that not only are the background levels the same (1.2 µA), but the deviation from the beam stimulation is nearly identical (+0.2 µA or −0.2 µA, respectively).

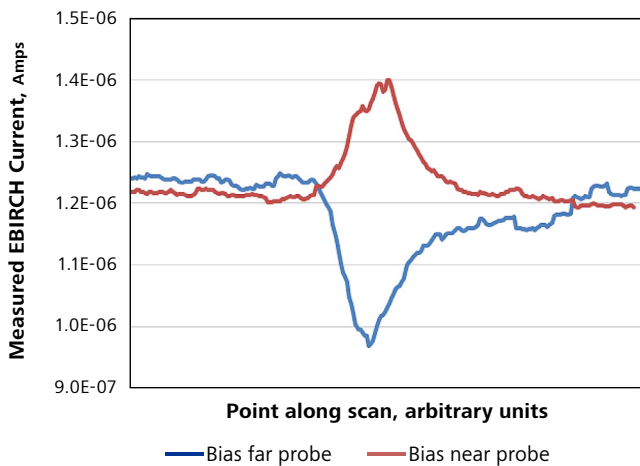## EBIRCH results across defect as function of bias

Figure 13 *Comparison of EBIRCH currents for two EBIRCH scans of same field of view, with probe bias either near or far.*

Previous literature [6] [7] has listed various mechanisms that could possibly play a role in EBIRCH or OBIRCH (Optical Beam Induced Resistance CHange). They are:

- Resistivity change as a function of temperature,
- Seebeck effect
- Thermal promotion of carriers
- The EBIC effect

It is clear that the last two would not be involved in a situation with an ohmic short, as they involve junctions. Of the first two mechanisms for EBIRCH, resistivity change should cause the same decrease/increase in both directions. But this is not the case. It is therefore assumed that this defect has created an ohmic short across two dissimilar materials (most likely being tungsten and silicon), and the heating provided by the SEM beam at the materials interface has provided an extra voltage according to the Seebeck effect. These results provide additional confirmation that Seebeck is one of the predominantdriving forces in EBIRCH analysis.

Conclusions

A systematic exploration of shorting currents was undertaken. Without creating an ohmic short, careful application of increasing stresses resulted in what would be called a soft failure in a 22 nm SRAM environment. EBIRCH analysis on a shorting current of roughly 12 nA was able to image fins at 2 kV SEM imaging. Stressing the sample at higher voltages eventually created an ohmic short, and "reduced" the sample to one spot. Next, variations of the gain and averaging were able to increase the current by 4X, providing a reminder of the importance of beam conditions. Finally, a careful consideration of how the current magnitudes are changed provides an affirmation of the Seebeck effect as a driving mechanism in EBIRCH.

References

[1]   S. Agarwal, ""Identifying EOS and EDS Failures in Semiconductor Devices"," Electronic Design, no. May 21, 2014.

[2]   J. F. Zeigler and e. al., "IBM Experiments in soft fails in computer electronics (1978-1994)," IBM J. Res. Develop., vol. 40, no. 1, 1996.

[3]   S. Yang and W. Wolf, "Case Study of Reliability-Aware and Low-Power Design," IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, vol. 16, no. 7, 2008.

[4]   G. Johnson, C. D'Aleo, Z. Xu, U. Kwon, H. Berman, Y. Feng, S. Darling, B. Yates, Y. Wang, M. Kagerer and R. Newton, "Electron Beam Induced Resistance Change for Device Characterization and Defect Localization," ISTFA, 2016.

[5]   G. Johnson, A. Rummel, M. Kemmler, T. Lundquist and B. Niu, "Probing SRAM Signals for Yield Management," IPFA, 2019.

[6]   K. Nikawa, "Method and system for testing an interconnection in a semiconductor integrated circuit," US Patent number 5,804,980.

[7]   G. M. Johnson, Z. Khan, C. D'Aleo, B. Yates, M. Iwatake and A. Katnani, "Beam-based defect localization using electrons: an EBIRCH overview," ISTFA, 2018.

Low-voltage EBIC Investigation of Fails

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Seeing beyond

Abstract

An investigation of shorting defects in SRAM structures by means of low-voltage EBIC is presented and the location of the defect was compared to the one isolated with EBIRCH. A pulldown device in 7 nm technology was intentionally overstressed, and the shorting location isolated with EBIRCH at 500 V. Then a series of EBIC investigations at very low voltage were undertaken in an experiment to isolate the problem. It was determined that some information about the nature of the defect was clear at beam landing energies as low as 150 V.

Introduction

This publication aims at achieving a complete understanding of failures that influence the quality of well and diffusion implants at very low beam voltages down to 70 V. It has been shown that electrical properties of a device under test (DUT) can be imaged using EBIC (Electron Beam Induced Current) by tuning the electron beam's acceleration voltage [1]. These properties were examined using beam voltages down to 500 V. The corresponding beam interaction volume is about 10 nm in diameter. As semiconductor devices shrink both horizontally and vertically, a smaller interaction volume between the electron beam and the sample is required in order to investigate current and future process nodes. Furthermore, there is an increasing concern that the beam interaction with the sample may alter the electrical properties or the nature of the defect [2,3,4] and thus any analytical technique which can use very low voltages is appreciated.

In this work we examined electrical properties of the active region by comparing EBIC images taken at different beam voltages before and after creating a failure.

Methods

Three electron beam induced methods were used in this work: EBIC, EBAC [5, 6] and EBIRCH Electron Beam Induce Resistance CHange). [7, 8, 9]. While EBIRCH requires two probe tips to be landed on two ends of the structure where a defect is assumed to be, EBIC and EBAC images can also be obtained using only one needle. For most applications the bulk contact has to be considered as an additional sink for or source of electrons.

For EBIRCH, one needle is biased and the other is grounded while the electron beam scans the area of interest. At defect sites, the incident electron beam will result in a change of resistance in the circuit. This change of resistance is measured and visualized simultaneously with the SE image in order to locate the defect. Tuning the electron beam's acceleration voltage provides access to various depths within the sample.

EBIC applications using one probe needle are used to visualize p-n junctions by detecting current that is the result of internal electric fields in the sample. The affected electrons include incident electrons from the beam, secondary electrons, and electron/hole pairs liberated in semiconductor materials.

Like EBIC, EBAC measures current; however, in contrast to EBIC, the current is several orders of magnitude smaller as only electrons from the incident electron beam that reach the probe needle through the connected metal network or by diffusion without being amplified by the electric fields of the sample are detected. As this work aims at EBIC analyses at beam voltages below 500 V only few electron hole pairs are generated yielding a significant contribution of EBAC electrons to the EBIC current.

It would be helpful to provide a reminder of some of the basic aspects of SRAM cells which will be drawn upon in further discussion. Figure 1 shows the locations of nFET and pFET devices in an SRAM. For this entire study, a pulldown device was investigated. Figure 2 depicts both a SEI view and a schematic of the device to be tested. In this study, for the initial overstress, probes were landed on the gate and drain contacts. For the remaining EBIC work, only the gate contact was used. The device has two nFET fins.
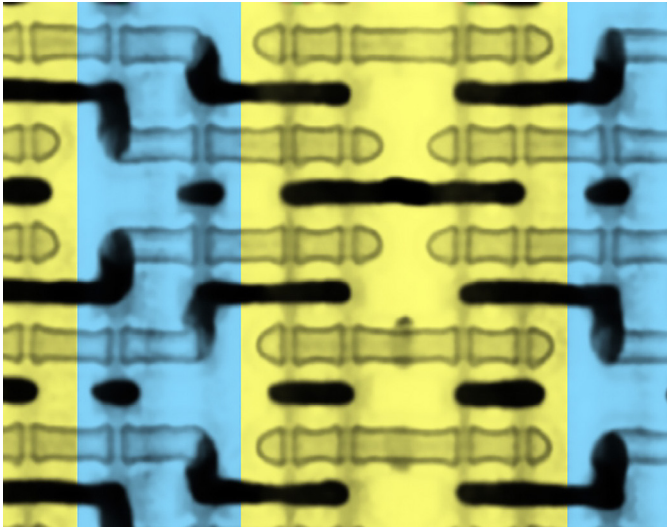
Figure 1 Pictorial view depicting nFET or P-well (yellow) and pFET or N-well (blue) regions of a typical SRAM sample. These are displayed as color coding of a backscattered image from a different chip polished to a deeper plane than used in this study.
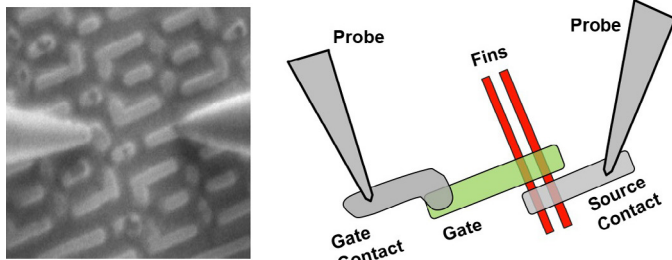

Figure 2 Pictorial view of structure under investigation, with the probes used for both the overstress operation and the subsequent EBIRCH analysis. Left, SE image Right, schematic view.

All analyzed images are taken with the same aperture of 30 µm. Potential artifacts by using different beam voltages have been neglected as it has been shown that the changes of electrical properties at even higher voltages are very slight [10].
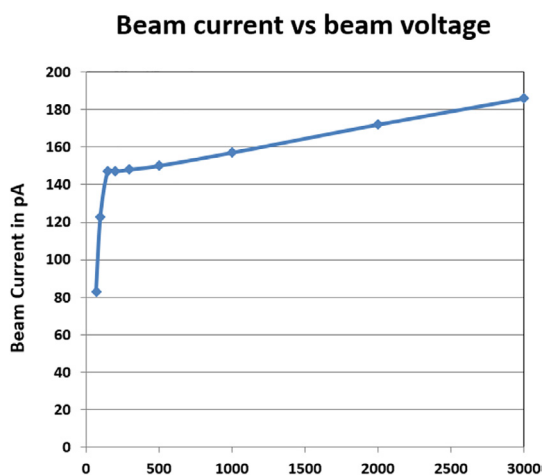

Figure 3 Measurements of beam current with a Faraday cup performed under identical conditions to those in this paper.

Results

The basic operations were:

- image the sample at a variety of acceleration potentials
- perform EBIC at a variety of acceleration potentials
- electrically overstress the sample
- perform EBIRCH at 500 V
- perform EBIC at a variety of acceleration potentials

SEI (Secondary Electron Images) collected with a GeminiSEM 300, at acceleration potentials of 70, 100, 150, 200, 300, and 500 V are shown in Figure 4. In these very high-resolution images, a gradual increase in the visibility of buried features is apparent. The 70 V image also demonstrates some slight passive voltage contrast in some of the blocks of the SRAM.
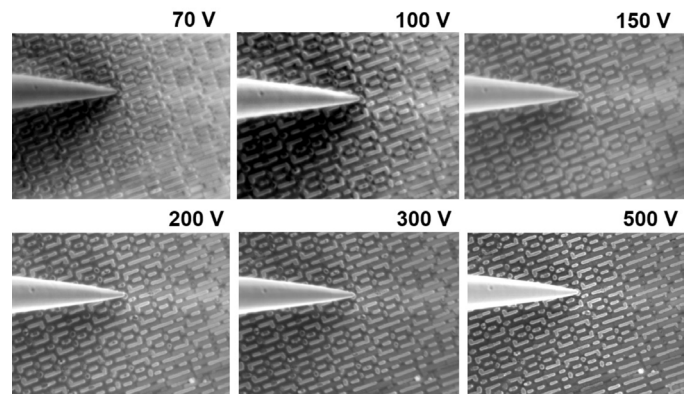

Figure 4 SE images taken at six different acceleration potential of a 7 nm SRAM with a GeminiSEM 300, showing excellent resolution, even below 100 V.

EBIC analysis with a PS8 nanoprober shuttle and EBIC module at these same voltages were also collected and displayed in Figure 5. As the acceleration potential increased the sample progressed from showing little EBIC, to very strong "white" signal at 150-500 V on the pFET regions, to a strong signal everywhere. The contrast was chosen such that currents leaving the probe (and thus the sample) were displayed as a white color. This contrast would be compatible with that expected for the passive voltage contrast effect between nFET and pFET contacts [11]. This provides further evidence that these effects are ultimately measuring secondary electron emission from the sample at various places.
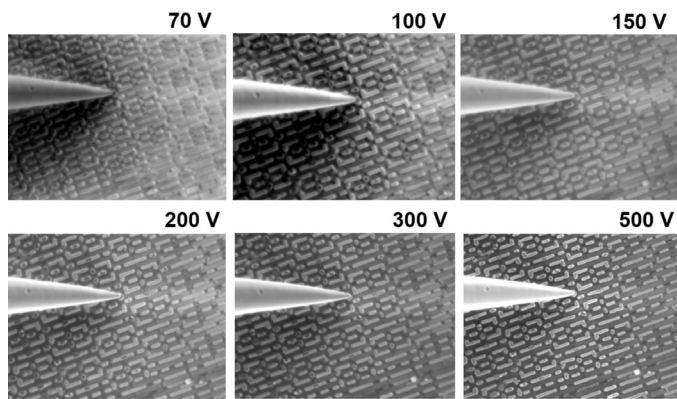
Figure 5 *EBIC images taken at six different acceleration potentials, before intentional overstress. The images show a progression from surface to deeper effects. pFET contacts light up very strongly under these conditions.*
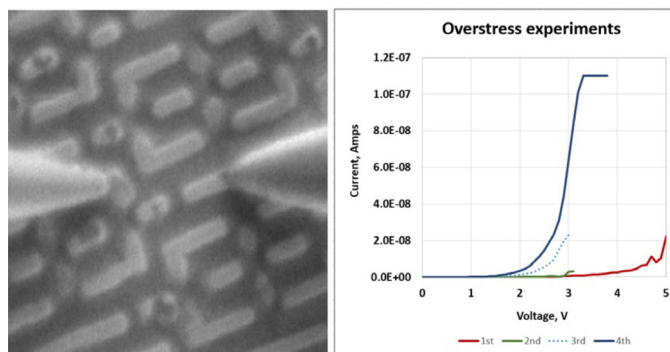

Figure 6 *SE image of gate/drain contacts in pulldown device (left), I-V curves taken during the analysis. A maximum of 160 nA was applied, and there is no evidence of any crater, giving strong indication that a small fail was created.*

Figure 7 *SEM with EBIRCH-overlay the sample after electrical stress. Note that there is no crater or blowout seen top-down in this image. EBIRCH shows spots near one fin and likely along a fin sidewall.*

Figure 8 *Post-blow EBIC images taken at a variety of acceleration potentials. The background signal is much higher than in Figure 3, which will be discussed in greater detail in the text.*

The sample next underwent an intentional overstress. With an appropriately low compliance setting, increasingly higher voltage between gate and drain contacts of a pulldown device was applied until a substantial increase in current was seen. For this device, a maximum current of 160 nA was applied. The SEM and I-V curves are shown in Figure 6.

Next, EBIRCH was performed on the device. SEM and EBIRCH images are displayed in Figure 4. EBIRCH was performed at several different beam landing energies: the strongest signal occurred at around 500 V beam landing energy. The location of the failure identified using EBRICH results in two close spots, one at the end of the contacted gate, the other close to the end around the transistor's second fin. Typically, EBIRCH spots tend to show a strong signal change at the location of the failure. In this case, a short was created that yielded a small EBIRCH signal without any features visible from topdown SEI inspection. Superimposing the EBIRCH data and the SE image with a high contrast setting and additional noise reduction filtering, a spot became clearly visible at the end of the gate. In addition, a smaller spot appeared at the position of the second fin.
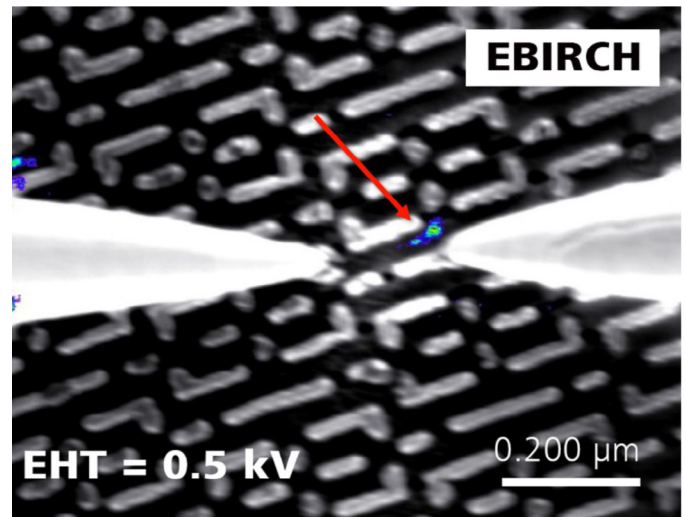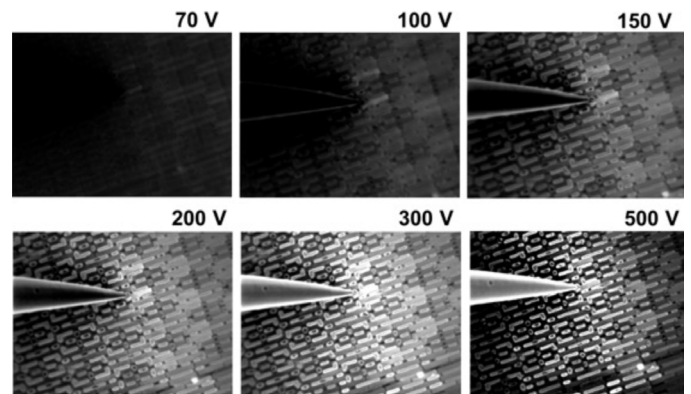
Afterwards, the same set of EBIC images were taken again and compared with the first set. These images are displayed in Figure 8. Once again, more features light up as the acceleration potential increases.

Presentation of Trends
Comparison to structure

In contrast to EBIRCH, where a maximum signal was obtained at a beam voltage of around 500 V, the EBIC images before and after generating a failure mainly differ at 150 V and 200 V. These are displayed in Figure 9. Even low kV EBIC yields information about the "diode health" in a neighborhood. For example, the EBIRCH image shows a spot which implies it is down the side, possibly to the well.

The EBIC experiment, undertaken very carefully at beam voltages as low as 70 V, but showing the best results at 150 V, demonstrates a change in the grounding state of the whole region. Before the blow, when contacting an internal node contact, we see only PFET devices in the region light up. As the figure shows, the NFET contacts (GND and BL) are dark. After the blow, all contacts in the region light up, thereby giving some diagnostic information that the short has likely gone to the well. It should be noted that the EBIC image showing the pre-blow seems to be less sharp than the post-blow image even though many structures are definitely in focus. This ehavior was not observed at other beam voltages.
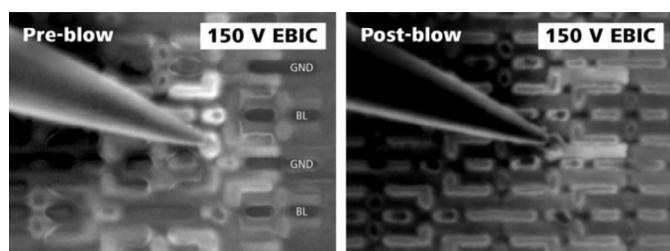

Figure 9 *Beam voltage 150 V, pre-blow left and post-blow right side, as-recorded EBIC images. The location of nFET contacts (Bitline and Ground) are overlaid in the image to highlight the contrast of each type. The post-blow image shows that most of these contacts now light up.*

Quantitative mapping

The utilized analysis software also provides the capability of quantitatively mapping the current across the sample, in this case on a scale of some 10's of pA. These results are displayed in Figure 10. Note that there is a shadow effect in the left half of the image due to reduced secondary electron emission because of the probe.
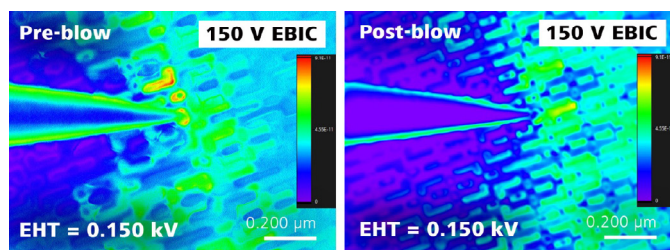

Figure 10 *Color maps quantitatively displaying the current absorbed at each pixel. The gate that has been probed stands out somewhat more strongly than its peers.*

Quantitative line scan

Quantitative measurements of the EBIC current along and across the gate show a current change before and after creating the failure. See Figure 11. The EBIC current at the failing gate is about 20% higher than the EBIC current across the neighboring gate.

Unlike the EBIRCH results, a clear spot could not be detected using EBIC. However, the maximum EBIC current measured along the direction, down the middle of the gate, is close to the two EBIRCH spots.
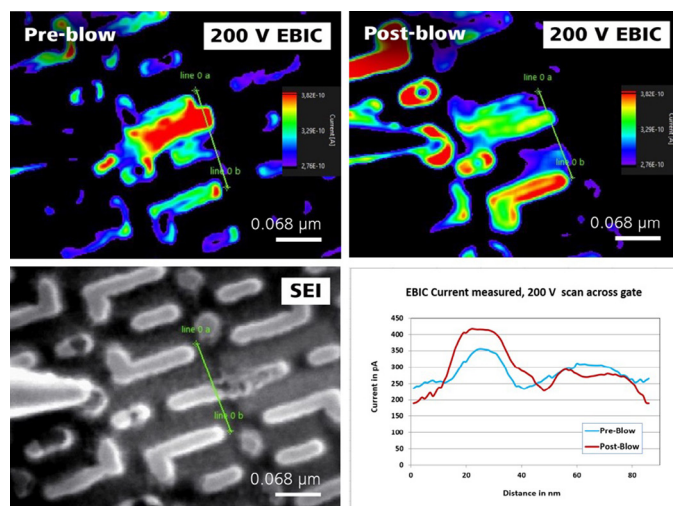

Figure 11 *EBIC current measured perpendicular to the gates, both before and after the intentional overstress, and including both the failing gate and an intact reference gate. The same color scale is used for each. The results demonstrate that after the overstress, the gate has 20% more current. This likely means that the gate is connected to a larger reservoir or shorted to more material.*
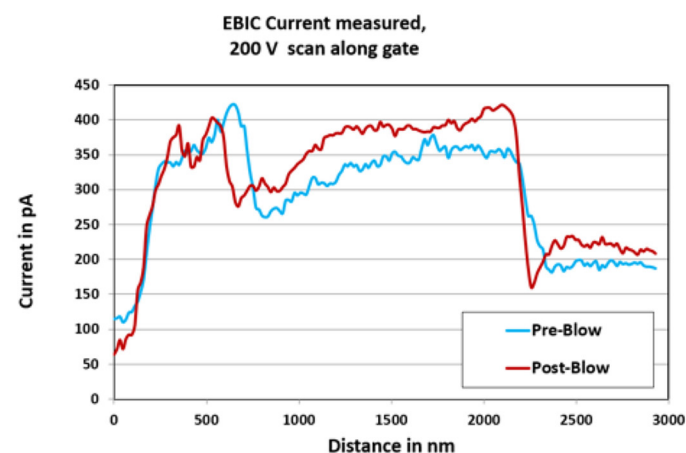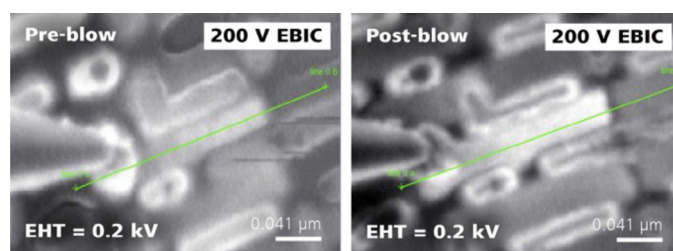

Figure 12 *EBIC current measured along the failing gate and a part of a following intact reference gate. Top views are EBIC images; graph numerically compares data along the scan.*

It should be noted that the current of the next gate following the failing gate was measured to be 10% higher, as shown in Figure 12. Nevertheless a significant increase of about 20% at the edge of the gate could be observed. Note that the pulldown device is a two-fin device. The higher current at the end of the gate gives an indication that the fin on the right is mostly likely failing and the one which would merit further physical analysis. Table 1 summarizes the results for 200 V imaging.

This work also demonstrates the capability of taking high resolution SE and EBIC images on a 7 nm device at very low beam voltages down to 70 V.

	Gate, over failing fin	Gate, over failing fin	Next gate, over fin (uncontacted)
Pre-Blow	350 pA	300 pA	200 pA
Post-Blow	420 pA	370 pA	220 pA

Table 1 *Numerical comparison of line scan data for various currents across the sample at 200 V.*

Discussion of Issues Raised
Differences in sensitivity
In contrast to the EBIRCH data, where a maximum signal was obtained at a beam voltage of around 500 V, the EBIC images before and after overstress mainly differ at 150 V and 200 V. One possible contributing factor is that the EBIRCH applies an external electrical field between the two probe tips that influences the incident beam's electrons. However, to fully understand this, it may be helpful to consider beam scattering and sample charging.

A Monte Carlo simulation [12] was calculated for electron scattering in silicon and is displayed in Figure 13. At 100 V, the electron scattering volume is about 1 nm in radius. Even at 500 V, the highest acceleration potential used in this study, the radius is closer to 5 nm. Thus, the beam is not directly interacting with the buried gates.
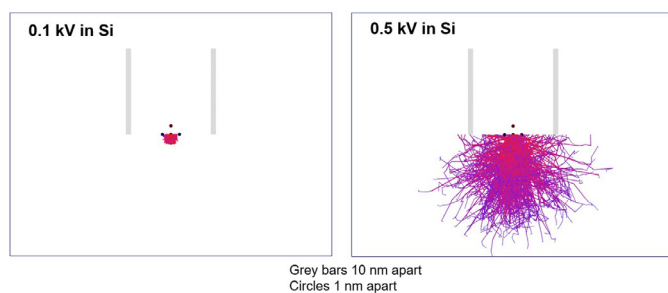

Figure 13 *Casino models for 100 and 500 V electron beam scattering in silicon.*

Next, the basic understanding of sample charging should be explored. Seiler [13] summarized this phenomena for various metals; the plot of the δ function in Figure 14 below is taken from this work. Below an energy EI, the sample will charge negative; above EI the sample will charge positive as a greater number of secondary electrons leave the sample. According to Seiler, the EI for several metals is ~300 eV, with tungsten reaching its maximum δ at an energy of 500 eV.

Earlier in the paper, this work established that the EBIC here was measuring a net loss of secondaries from the sample. If the acceleration potential is sufficiently low, there is a net retardation of the effect due to irregularities of the sample. This work proposes that the retardation allows the analyst to pick out sensitive details in the sample. As we have seen, at high kV, everything emits, and we have no information.

Do the EBIC results correlate with the EBIRCH results?
In order to compare the EBIC and EBIRCH results, both images' contrast and brightness of was increased such that only the highest currents were displayed in Figure 15. Comparing the two images shows a reasonably good correlation. A correlation between the EBIC image at 150 V and the EBIRCH image at 500 V definitely exists although the changes in current are small.

A conceptual diagram is displayed in Figure 16. The left image shows an overlay of our EBIC data to a SEM micrograph of a different chip examined in backscatter imaging. The right image is a cartoon of the expected short. It is believed that the fin further away from the contact is predominantly responsible for the leakage.
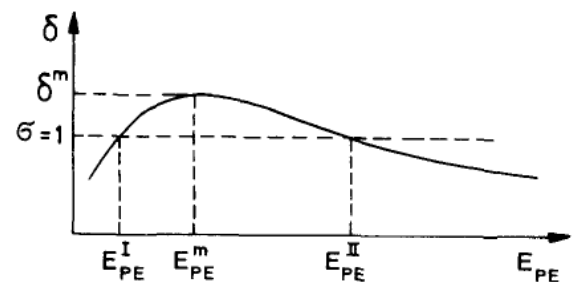

Figure 14 *Plot of Secondary electron yield (δ) as a function of primary electron beam, from Seiler. At EI, the sample has no net or loss of electrons. Above EI, the sample charges positive.*

Figure 15 *Comparison of EBIRCH, EBIC, and overlay of the two data sets. In the left image, EBIRCH data are overlaid with green; in the right EBIC is overlaid in red.*
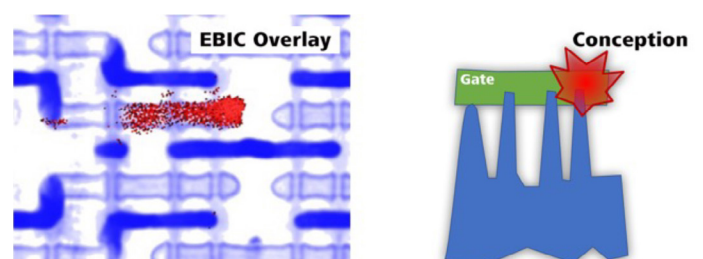

Figure 16 *Left: Overlay of EBIC data (red) from this analysis with BSE image of similar devices (blue); cartoon depicting model for fail that unites both data (right).*

How can the correlation between EBIC images and EBIRCH images at different voltages be explained?

For example, the EBIRCH image shows a spot which implies it is down the side, possibly to the well. The EBIC, undertaken very carefully at beam voltages as low as 70 V, but showing most excellent results at 150 V, demonstrates a change in the grounding state of the whole region. Before the blow, when contacting an internal node contact, we see only PFET devices in the region light up. As the figure on the left shows, the NFET contacts (GND and BL) are dark. After the blow, all contacts in the region light up, thereby giving some diagnostic information that the short has likely gone to the well.

What is the influence of absorbed electrons (EBAC) to the electrons generated in a p-n junction (EBIC)?

A look at the images of Figure 5 and Figure 8 shows that with higher voltage a larger area becomes visible. In order to reach the probe needle these EBIC electrons from this area are generated in the active region and mainly contribute to the image. EBAC electrons are reaching the probe needle directly through connected metal or poly lines. However, even at beam voltages of 150 V and less we can see that also electrons from a neighbouring contact are detected by the amplifier which is not possible for EBAC electrons as the neighbouring transistor contact is insulated from the contacted one.

Future Work

This work represented a first attempt to correlate EBIC and EBIRCH imaging at very low kV. Additional analyses are planned to investigate further using different current compliances to have clearer signals. In addition, STEM or TEM analysis are planned.

Reference

[1] G. Johnson, J. Saujauddin, T. Rodgers and J. Lee, "Characterization of electronic devices by top-down Electron Beam Induced Current," *IPFA,* pp. pp. 1-5, 2020.

[2] E. Cole, ""Beam-Based Defect Localization Techniques"," *ISTFA,* vol. Tutorials, 2007.

[3] N. J. Saujauddin, T. Niemi, T. Lundquist and B. Niu, "Electrical Probing of 7nm SRAMS/SOC at Contact Layer," *ISTFA,* 2020.

[4] Y.-X. Chen, P.-N. Hsu, Y.-M. Chung, H.-C. Hsu, H.-S. Ku, C.-C. Yeh, N.-T. Lian, T. Yang, K.-C. Chen and C.-Y. Lu, "A Discussion of Dielectric Film Deformation by E-Beam Energy," *ISTFA,* 2018.

[5] M. Simon-Najasek, J. Jatzkowsk, C. Große and F. Altmann, "A New Technique for Non-Invasive Short-Localisation in Thin Dielectric Layers by Electron Beam Absorbed Current (EBAC) Imaging," *ISTFA,* 2012.

[6] D. Dahanayaka, D. Bader, D. Prevost, M. Coster, E. Mccullen, M. Masters and K. Stevens, ""Intra-Device Defect Localization through EBIC/EBAC Combined with Electrical Nano-Probing for FinFET Devices Composed of Multiple Sub-Elements","*ISTFA,*, 2016.

[7] K. Nikawa, "Method and system for testing an interconnection in a semiconductor integrated circuit," *US Patent number 5,804,980.*

[8] B. Buchea, H. Ryu, M. v. Haartman, C. Butler and T. Tong, "High Resolution Electron Beam Induced Resistance Change for Fault Isolation with 100nm^2 Localization," *ISTFA,* 2016.

[9] G. Johnson, C. D'Aleo, Z. Xu, U. Kwon, H. Berman, Y. Feng, S. Darling, B. Yates, Y. Wang, M. Kagerer and R. Newton, "Electron Beam Induced Resistance Change for Device Characterization and Defect Localization," *ISTFA,* 2016.

[10] N. J. Saujauddin, E. P. Y. Chen and F. Beaudoin, "Nanoprobing beyond 14 nm with latest generation SEM-based nano-probers," *ISTFA,* 2017.

[11] R. Rosenkranz, ""Failure localization with active and passive voltage contrast in FIB and SEM"," *Journal of Materials Science-materials in Electronics,* 2011.

[12] D. Drouin, A. Couture, D. Joly, N. Poirier-Demers and a. H. Demers, "monte CArlo SImulation of electroN trajectory in sOlids, Casino Version 3.3.0.4," 2016.

[13] H. Seiler, ""Secondary electron emission in the scanning electron microscope," J*ournal of Applied Physics,* vol. 54, no. R1, 1983.

[14] A. J. Smith, A. Rummel, M. Kemmler, K. Schock and S. Kleindiek, "Locating low-ohmic Variations in Resistance using Electron Beam Induced Voltage Imaging," *ISTFA,* 2020.

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